

	Document ID	U	Title	Current OR
164	US 51758 62 A	<input checked="" type="checkbox"/>	Method and apparatus for a special purpose arithmetic boolean unit	712/7
165	US 51596 86 A	<input checked="" type="checkbox"/>	Multi-processor computer system having process-independent communication register addressing	718/105
166	US 51519 95 A	<input checked="" type="checkbox"/>	Method and apparatus for producing successive calculated results in a high-speed computer functional unit using low-speed VLSI components	713/501
167	US 51485 44 A	<input checked="" type="checkbox"/>	Apparatus and method for control of asynchronous program interrupt events in a data processing system	710/261
168	US 51270 93 A	<input checked="" type="checkbox"/>	Computer look-ahead instruction issue control	712/217
169	US 51230 95 A	<input checked="" type="checkbox"/>	Integrated scalar and vector processors with vector addressing by the scalar processor	712/218
170	US 50864 98 A	<input checked="" type="checkbox"/>	Parallel computer with asynchronous communication facility	709/236
171	US 50864 08 A	<input checked="" type="checkbox"/>	Method and apparatus for merging	707/200
172	US 50634 97 A	<input checked="" type="checkbox"/>	Apparatus and method for recovering from missing page faults in vector data processing operations	712/6
173	US 50601 48 A	<input checked="" type="checkbox"/>	Control system for vector processor with serialization instruction for memory accesses for pipeline operation	712/6
174	US 50500 70 A	<input checked="" type="checkbox"/>	Multi-processor computer system having self-allocating processors	712/203
175	US 50142 35 A	<input checked="" type="checkbox"/>	Convolution memory	708/520
176	US 50017 01 A	<input checked="" type="checkbox"/>	Subband echo canceler including real time allocation among the subbands	370/290
177	US 49910 83 A	<input checked="" type="checkbox"/>	Method and system for extending address space for vector processing	711/207
178	US 49568 00 A	<input checked="" type="checkbox"/>	Arithmetic operation processing apparatus of the parallel processing type and compiler which is used in this apparatus	708/524
179	US 49567 67 A	<input checked="" type="checkbox"/>	Data processing system with model for status accumulating operation by simulating sequence of arithmetic steps performed by arithmetic processor	703/13
180	US 48992 73 A	<input checked="" type="checkbox"/>	Circuit simulation method with clock event suppression for debugging LSI circuits	703/14
181	US 48902 20 A	<input checked="" type="checkbox"/>	Vector processing apparatus for incrementing indices of vector operands of different length according to arithmetic operation results	712/8
182	US 48886 79 A	<input checked="" type="checkbox"/>	Method and apparatus using a cache and main memory for both vector processing and scalar processing by prefetching cache blocks including vector data elements	712/6
183	US 48736 30 A	<input checked="" type="checkbox"/>	Scientific processor to support a host processor referencing common memory	712/3
184	US 48377 30 A	<input checked="" type="checkbox"/>	Linking scalar results directly to scalar operation inputs on a bidirectional databus in a computer which superpositions vector and scalar operations	712/7
185	US 47915 55 A	<input checked="" type="checkbox"/>	Vector processing unit	712/1
186	US 47854 00 A	<input checked="" type="checkbox"/>	Method for processing a data base	707/100

	L #	Hits	Search Text	DBs
1	L1	396	(shar\$3 common unified united combin\$3 mode) near20 (scalar near10 (vector pack\$3 simd))	USPAT; US_PGPUB
2	L2	9791	(tag bit field flag indicat\$3 identif\$6) near30 ((activ\$5 valid\$4 enabl\$3 disabl\$3 invalid\$4 set\$4) near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	USPAT; US_PGPUB
3	L3	72	1 and 2	USPAT; US_PGPUB
4	L5	1285	(tag bit field flag indicat\$3 identif\$6) near30 ((activ\$5 valid\$4 enabl\$3 disabl\$3 invalid\$4 set\$4) near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	EPO; JPO; DERWENT; IBM_TDB
5	L6	0	4 and 5	EPO; JPO; DERWENT; IBM_TDB
6	L4	74	(shar\$3 common unified united combin\$3 mode) near20 (scalar near10 (vector pack\$3 simd))	EPO; JPO; DERWENT; IBM_TDB

	Document ID	U	Title	Current OR
1	US 20030 15902 3 A1	<input type="checkbox"/>	Repeated instruction execution	712/241
2	US 20030 07909 0 A1	<input checked="" type="checkbox"/>	Instructions for test & set with selectively enabled cache invalidate	711/140
3	US 20030 03722 1 A1	<input checked="" type="checkbox"/>	Processor implementation having unified scalar and SIMD datapath	712/3
4	US 20030 03350 6 A1	<input checked="" type="checkbox"/>	Locking source registers in a data processing apparatus	712/217
5	US 20020 11618 6 A1	<input checked="" type="checkbox"/>	Voice activity detector for integrated telecommunications processing	704/233
6	US 20020 07603 4 A1	<input checked="" type="checkbox"/>	Tone detection for integrated telecommunications processing	379/390 .02
7	US 20020 06413 9 A1	<input checked="" type="checkbox"/>	Network echo canceller for integrated telecommunications processing	370/289
8	US 20020 03284 8 A1	<input checked="" type="checkbox"/>	Method and apparatus for obtaining a scalar value directly from a vector register	712/4
9	US 20020 02656 9 A1	<input checked="" type="checkbox"/>	Method and apparatus for efficient loading and storing of vectors	712/4
10	US 66752 85 B1	<input checked="" type="checkbox"/>	Geometric engine including a computational module without memory contention	712/201
11	US 66402 99 B1	<input checked="" type="checkbox"/>	Method and apparatus for arbitrating access to a computational engine for use in a video graphics controller	712/245
12	US 66309 35 B1	<input checked="" type="checkbox"/>	Geometric engine including a computational module for use in a video graphics controller	345/522
13	US 66248 18 B1	<input checked="" type="checkbox"/>	Method and apparatus for shared microcode in a multi-thread computation engine	345/522
14	US 65670 84 B1	<input checked="" type="checkbox"/>	Lighting effect computation circuit and method therefore	345/426
15	US 65570 96 B1	<input checked="" type="checkbox"/>	Processors with data typer and aligner selectively coupling data bits of data buses to adder and multiplier functional blocks to execute instructions with flexible data types	712/221
16	US 63518 01 B1	<input checked="" type="checkbox"/>	Program counter update mechanism	712/205
17	US 60887 83 A	<input checked="" type="checkbox"/>	DPS having a plurality of like processors controlled in parallel by an instruction word, and a control processor also controlled by the instruction word	712/22
18	US 60852 75 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	710/316
19	US 60471 22 A	<input checked="" type="checkbox"/>	System for method for performing a context switch operation in a massively parallel computer system	718/108
20	US 60353 86 A	<input checked="" type="checkbox"/>	Program counter update mechanism	712/205

	Document ID	U	Title	Current OR
21	US 60163 95 A	<input checked="" type="checkbox"/>	Programming a vector processor and parallel programming of an asymmetric dual multiprocessor comprised of a vector processor and a risc processor	717/149
22	US 59266 43 A	<input checked="" type="checkbox"/>	Data driven processor performing parallel scalar and vector processing	712/7
23	US 58226 06 A	<input checked="" type="checkbox"/>	DSP having a plurality of like processors controlled in parallel by an instruction word, and a control processor also controlled by the instruction word	712/16
24	US 58058 74 A	<input checked="" type="checkbox"/>	Method and apparatus for performing a vector skip instruction in a data processor	712/222
25	US 57991 62 A	<input checked="" type="checkbox"/>	Program counter update mechanism	712/205
26	US 57548 05 A	<input checked="" type="checkbox"/>	Instruction in a data processing system utilizing extension bits and method therefor	712/200
27	US 57520 74 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	712/29
28	US 57457 21 A	<input checked="" type="checkbox"/>	Partitioned addressing apparatus for vector/scalar registers	712/208
29	US 57427 86 A	<input checked="" type="checkbox"/>	Method and apparatus for storing vector data in multiple non-consecutive locations in a data processor using a mask value	711/217
30	US 57402 83 A	<input checked="" type="checkbox"/>	Digital video compression utilizing mixed vector and scalar outputs	382/248
31	US 57375 86 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	712/236
32	US 57348 79 A	<input checked="" type="checkbox"/>	Saturation instruction in a data processor	712/221
33	US 57179 47 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	712/3
34	US 57178 81 A	<input checked="" type="checkbox"/>	Data processing system for processing one and two parcel instructions	712/205
35	US 57064 90 A	<input checked="" type="checkbox"/>	Method of processing conditional branch instructions in scalar/vector processor	712/234
36	US 57064 88 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	712/223
37	US 56896 47 A	<input checked="" type="checkbox"/>	Parallel computing system with processing element number setting mode and shortest route determination with matrix size information	712/11
38	US 56690 13 A	<input checked="" type="checkbox"/>	System for transferring M elements X times and transferring N elements one time for an array that is X*M+N long responsive to vector type instructions	710/5
39	US 56665 35 A	<input checked="" type="checkbox"/>	Microprocessor and data flow microprocessor having vector operation function	718/104
40	US 56641 34 A	<input checked="" type="checkbox"/>	Data processor for performing a comparison instruction using selective enablement and wired boolean logic	712/245
41	US 56597 06 A	<input checked="" type="checkbox"/>	Vector/scalar processor with simultaneous processing and instruction cache filling	711/125
42	US 56550 96 A	<input checked="" type="checkbox"/>	Method and apparatus for dynamic scheduling of instructions to ensure sequentially coherent data in a processor employing out-of-order execution	712/200
43	US 56405 24 A	<input checked="" type="checkbox"/>	Method and apparatus for chaining vector instructions	712/222

	Document ID	U	Title	Current OR
44	US 56236 85 A	<input checked="" type="checkbox"/>	Vector register validity indication to handle out-of-order element arrival for a vector computer with variable memory latency	712/9
45	US 56236 50 A	<input checked="" type="checkbox"/>	Method of processing a sequence of conditional vector IF statements	712/234
46	US 56008 46 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	712/5
47	US 55985 71 A	<input checked="" type="checkbox"/>	Data processor for conditionally modifying extension bits in response to data processing instruction execution	712/9
48	US 55985 47 A	<input checked="" type="checkbox"/>	Vector processor having functional unit paths of differing pipeline lengths	712/222
49	US 55726 89 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	712/200
50	US 55617 84 A	<input checked="" type="checkbox"/>	Interleaved memory access system having variable-sized segments logical address spaces and means for dividing/mapping physical address into higher and lower order addresses	711/157
51	US 55599 75 A	<input checked="" type="checkbox"/>	Program counter update mechanism	712/230
52	US 55599 73 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	712/241
53	US 55487 68 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	712/200
54	US 55443 37 A	<input checked="" type="checkbox"/>	Vector processor having registers for control by vector registers	712/4
55	US 55375 62 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	712/234
56	US 54715 93 A	<input checked="" type="checkbox"/>	Computer processor with an efficient means of executing many instructions simultaneously	712/235
57	US 54308 84 A	<input checked="" type="checkbox"/>	Scalar/vector processor	712/3
58	US 54045 53 A	<input checked="" type="checkbox"/>	Microprocessor and data flow microprocessor having vector operation function	712/25
59	US 53613 63 A	<input checked="" type="checkbox"/>	Input/output system for parallel computer for performing parallel file transfers between selected number of input/output devices and another selected number of processing nodes	712/22
60	US 53534 12 A	<input checked="" type="checkbox"/>	Partition control circuit for separately controlling message sending of nodes of tree-shaped routing network to divide the network into a number of partitions	709/243
61	US 53496 77 A	<input checked="" type="checkbox"/>	Apparatus for calculating delay when executing vector tailgating instructions and using delay to facilitate simultaneous reading of operands from and writing of results to same vector register	712/4
62	US 53333 20 A	<input checked="" type="checkbox"/>	Electronic computer system and processor element used with the computer system	713/100
63	US 53332 91 A	<input checked="" type="checkbox"/>	Stride enhancer for high speed memory accesses with line fetching mode and normal mode employing boundary crossing determination	711/157
64	US 51971 30 A	<input checked="" type="checkbox"/>	Cluster architecture for a highly parallel scalar/vector multiprocessor system	712/3
65	US 51758 62 A	<input checked="" type="checkbox"/>	Method and apparatus for a special purpose arithmetic boolean unit	712/7

	Document ID	U	Title	Current OR
66	US 50739 70 A	<input checked="" type="checkbox"/>	Vector processing apparatus allowing succeeding vector instruction chain processing upon completion of decoding of a preceding vector instruction chain	712/7
67	US 49741 98 A	<input checked="" type="checkbox"/>	Vector processing system utilizing firm ware control to prevent delays during processing operations	712/8
68	US 49640 35 A	<input checked="" type="checkbox"/>	Vector processor capable of high-speed access to processing results from scalar processor	712/3
69	US 49454 79 A	<input checked="" type="checkbox"/>	Tightly coupled scientific processing system	712/3
70	US 48377 30 A	<input checked="" type="checkbox"/>	Linking scalar results directly to scalar operation inputs on a bidirectional databus in a computer which superpositions vector and scalar operations	712/7
71	US 47775 93 A	<input checked="" type="checkbox"/>	Vector processing apparatus including means for identifying the occurrence of exceptions in the processing of vector elements	712/9
72	US 46333 89 A	<input type="checkbox"/>	Vector processor system comprised of plural vector processors	712/4

	L #	Hits	Search Text	DBs
24	L39	52306	((activ\$5 valid\$4 enable\$3 disable\$3 invalid\$4 set\$4) near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	USPAT; US-PGPUB
25	L40	781	((sav\$3 reduce\$4 lower\$3) near10 (energy power)) and (scalar near20 (vector SIMD packed))	USPAT; US-PGPUB
26	L41	320	((sav\$3 reduce\$4 lower\$3) near10 (energy power)) near50 39	USPAT; US-PGPUB
27	L42	4	41 and (scalar near20 (vector SIMD packed))	USPAT; US-PGPUB
28	L43	133	40 and ((activ\$5 valid\$4 enable\$3 disable\$3 invalid\$4 set\$4) near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	USPAT; US-PGPUB
29	L44	404	(scalar near50 (vector SIMD packed)) near20 (alu (datapath (data adj1 path)) ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	USPAT; US-PGPUB
30	L45	21	40 and 44 /	USPAT; US-PGPUB
31	L49	628	(vector SIMD packed) near10 (plural plurality number several two multiple multiplicity) adj5 (alu (datapath (data adj1 path)) ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	USPAT; US-PGPUB
32	L51	709	scalar near10 (alu (datapath (data adj1 path)) ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	USPAT; US-PGPUB
33	L53	53	49 near99 51	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
187	US 47808 11 A	<input checked="" type="checkbox"/>	Vector processing apparatus providing vector and scalar processor synchronization	712/3
188	US 47791 92 A	<input checked="" type="checkbox"/>	Vector processor with a synchronously controlled operand fetch circuits	712/8
189	US 47776 15 A	<input checked="" type="checkbox"/>	Backplane structure for a computer superpositioning scalar and vector operations	710/300
190	US 47605 18 A	<input checked="" type="checkbox"/>	Bi-directional databus system for supporting superposition of vector and scalar operations in a computer	710/107
191	US 47408 94 A	<input checked="" type="checkbox"/>	Computing processor with memoryless function units each connected to different part of a multiported memory	711/149
192	US 47408 93 A	<input checked="" type="checkbox"/>	Method for reducing the time for switching between programs	712/222
193	US 47363 35 A	<input checked="" type="checkbox"/>	Multiplier-accumulator circuit using latched sums and carries	708/626
194	US 46444 71 A	<input checked="" type="checkbox"/>	Method for processing a data base	707/3
195	US 46333 89 A	<input checked="" type="checkbox"/>	Vector processor system comprised of plural vector processors	712/4
196	US 45410 46 A	<input checked="" type="checkbox"/>	Data processing system including scalar data processor and vector data processor	712/3
197	US 42451 82 A	<input checked="" type="checkbox"/>	Excitation control apparatus for a generator	322/20
198	US 41288 80 A	<input type="checkbox"/>	Computer vector register processing	712/4

	Document ID	U	Title	Current OR
1	US 20040 03995 2 A1	<input type="checkbox"/>	Method and apparatus for power reduction in a digital signal processor integrated circuit	713/300
2	US 20030 23351 3 A1	<input checked="" type="checkbox"/>	Information processing system and cache flash control method used for the same	711/103
3	US 20030 17224 9 A1	<input checked="" type="checkbox"/>	Methods of performing DSP operations with complex data type operands	712/35
4	US 20030 15441 9 A1	<input checked="" type="checkbox"/>	Register renaming in binary translation using rollback and recovery	714/2
5	US 20030 15436 0 A1	<input checked="" type="checkbox"/>	Methods of performing DSP operations using flexible data type operands	712/210
6	US 20030 14033 5 A1	<input checked="" type="checkbox"/>	Tracking format of registers having multiple content formats in binary translation	717/140
7	US 20030 13534 0 A1	<input checked="" type="checkbox"/>	User defined processing function	702/68
8	US 20030 12509 1 A1	<input checked="" type="checkbox"/>	Signal processing method and apparatus for obtaining diversity gain in wireless communication system equipping antenna array	455/562 .1
9	US 20030 09100 7 A1	<input checked="" type="checkbox"/>	User equipment and base station performing data detection using a scalar array	370/335
10	US 20030 08875 5 A1	<input checked="" type="checkbox"/>	Method and apparatus for the data-driven synchronous parallel processing of digital data	712/25
11	US 20030 08096 3 A1	<input checked="" type="checkbox"/>	High performance low cost video game system with coprocessor providing high speed efficient 3D graphics and digital audio signal processing	345/501
12	US 20030 05613 4 A1	<input checked="" type="checkbox"/>	Method and apparatus for power reduction in a digital signal processor integrated circuit	713/324
13	US 20020 18448 0 A1	<input checked="" type="checkbox"/>	Vectorized table lookup	712/300
14	US 20020 15225 3 A1	<input checked="" type="checkbox"/>	System and method for adaptive filtering	708/520
15	US 20020 14406 1 A1	<input checked="" type="checkbox"/>	Vector and scalar data cache for a vector multiprocessor	711/126
16	US 20020 08784 6 A1	<input checked="" type="checkbox"/>	Reconfigurable processing system and method	712/229
17	US 20020 08086 3 A1	<input checked="" type="checkbox"/>	Adaptive generalized matched filter rake receiver system and method	375/152

	Document ID	U	Title	Current OR
18	US 20020 07093 9 A1	<input checked="" type="checkbox"/>	Coding and decoding three-dimensional data	345/473
19	US 20020 03284 8 A1	<input checked="" type="checkbox"/>	Method and apparatus for obtaining a scalar value directly from a vector register	712/4
20	US 20020 02656 9 A1	<input checked="" type="checkbox"/>	Method and apparatus for efficient loading and storing of vectors	712/4
21	US 20020 00744 9 A1	<input checked="" type="checkbox"/>	Vector scatter instruction control circuit and vector architecture information processing equipment	712/4
22	US 67014 24 B1	<input checked="" type="checkbox"/>	Method and apparatus for efficient loading and storing of vectors	712/35
23	US 66970 76 B1	<input checked="" type="checkbox"/>	Method and apparatus for address re-mapping	345/568
24	US 66936 43 B1	<input checked="" type="checkbox"/>	Method and apparatus for color space conversion	345/602
25	US 66751 87 B1	<input checked="" type="checkbox"/>	Pipelined linear array of processor elements for performing matrix computations	708/622
26	US 66657 74 B2	<input checked="" type="checkbox"/>	Vector and scalar data cache for a vector multiprocessor	711/118
27	US 65939 29 B2	<input checked="" type="checkbox"/>	High performance low cost video game system with coprocessor providing high speed efficient 3D graphics and digital audio signal processing	345/501
28	US 65875 99 B1	<input checked="" type="checkbox"/>	Method and apparatus for producing a composed output resembling an image	382/284
29	US 65738 46 B1	<input checked="" type="checkbox"/>	Method and apparatus for variable length decoding and encoding of video streams	341/67
30	US 65713 28 B2	<input checked="" type="checkbox"/>	Method and apparatus for obtaining a scalar value directly from a vector register	712/35
31	US 65598 48 B2	<input checked="" type="checkbox"/>	Coding and decoding three-dimensional data	345/473
32	US 65570 96 B1	<input checked="" type="checkbox"/>	Processors with data typer and aligner selectively coupling data bits of data buses to adder and multiplier functional blocks to execute instructions with flexible data types	712/221
33	US 65561 97 B1	<input checked="" type="checkbox"/>	High performance low cost video game system with coprocessor providing high speed efficient 3D graphics and digital audio signal processing	345/419
34	US 65162 13 B1	<input checked="" type="checkbox"/>	Method and apparatus to estimate location and orientation of objects during magnetic resonance imaging	600/424
35	US 64969 02 B1	<input checked="" type="checkbox"/>	Vector and scalar data cache for a vector multiprocessor	711/118
36	US 64666 92 B1	<input checked="" type="checkbox"/>	Method and apparatus for processing visual information	382/156
37	US 64461 98 B1	<input checked="" type="checkbox"/>	Vectorized table lookup	712/300
38	US 64003 06 B1	<input checked="" type="checkbox"/>	Multi-channel moving target radar detection and imaging apparatus and method	342/25

	Document ID	U	Title	Current OR
39	US 63428 92 B1	<input checked="" type="checkbox"/>	Video game system and coprocessor for video game system	345/503
40	US 63318 56 B1	<input checked="" type="checkbox"/>	Video game system with coprocessor providing high speed efficient 3D graphics and digital audio signal processing	345/503
41	US 63174 66 B1	<input checked="" type="checkbox"/>	Wireless communications system having a space-time architecture employing multi-element antennas at both the transmitter and receiver	375/267
42	US 63083 16 B1	<input checked="" type="checkbox"/>	Apparatus for analyzing operations of parallel processing system	717/127
43	US 62791 52 B1	<input checked="" type="checkbox"/>	Apparatus and method for high-speed memory access	717/150
44	US 62753 11 B1	<input checked="" type="checkbox"/>	Optical device for processing an optical digital signal	359/107
45	US 62398 10 B1	<input checked="" type="checkbox"/>	High performance low cost video game system with coprocessor providing high speed efficient 3D graphics and digital audio signal processing	345/420
46	US 61756 63 B1	<input checked="" type="checkbox"/>	Method and apparatus for preserving background continuity in images	382/284
47	US 61667 48 A	<input checked="" type="checkbox"/>	Interface for a high performance low cost video game system with coprocessor providing high speed efficient 3D graphics and digital audio signal processing	345/522
48	US 61154 80 A	<input checked="" type="checkbox"/>	Method and apparatus for processing visual information	382/103
49	US 60852 75 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	710/316
50	US 60498 39 A	<input checked="" type="checkbox"/>	Data processor with multiple register queues	710/1
51	US 60121 35 A	<input checked="" type="checkbox"/>	Computer having multiple address ports, each having logical address translation with base and limit memory management	711/208
52	US 59915 31 A	<input checked="" type="checkbox"/>	Scalable width vector processor architecture for efficient emulation	703/26
53	US 59464 96 A	<input checked="" type="checkbox"/>	Distributed vector architecture	712/2
54	US 59266 43 A	<input checked="" type="checkbox"/>	Data driven processor performing parallel scalar and vector processing	712/7
55	US 59130 69 A	<input checked="" type="checkbox"/>	Interleaving memory in distributed vector architecture multiprocessor system	712/2
56	US 58902 22 A	<input checked="" type="checkbox"/>	Method and system for addressing registers in a data processing unit in an indirect addressing mode	711/220
57	US 58871 82 A	<input checked="" type="checkbox"/>	Multiprocessor system with vector pipelines	712/2
58	US 58450 16 A	<input checked="" type="checkbox"/>	Image compressing apparatus	382/253
59	US 58325 33 A	<input checked="" type="checkbox"/>	Method and system for addressing registers in a data processing unit in an indexed addressing mode	711/2
60	US 58260 96 A	<input checked="" type="checkbox"/>	Minimal instruction set computer architecture and multiple instruction issue method	712/24
61	US 58058 74 A	<input checked="" type="checkbox"/>	Method and apparatus for performing a vector skip instruction in a data processor	712/222

	Document ID	U	Title	Current OR
62	US 57684 45 A	<input checked="" type="checkbox"/>	Compression and decompression scheme performed on shared workstation memory by media coprocessor	382/305
63	US 57548 05 A	<input checked="" type="checkbox"/>	Instruction in a data processing system utilizing extension bits and method therefor	712/200
64	US 57520 74 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	712/29
65	US 57428 42 A	<input checked="" type="checkbox"/>	Data processing apparatus for executing a vector operation under control of a master processor	712/3
66	US 57427 86 A	<input checked="" type="checkbox"/>	Method and apparatus for storing vector data in multiple non-consecutive locations in a data processor using a mask value	711/217
67	US 57375 86 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	712/236
68	US 57348 79 A	<input checked="" type="checkbox"/>	Saturation instruction in a data processor	712/221
69	US 57200 05 A	<input checked="" type="checkbox"/>	Circuit and method for processing lower limit value fuzzy inputs during a fuzzy logic operation	706/1
70	US 57179 47 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	712/3
71	US 57178 95 A	<input checked="" type="checkbox"/>	Associative scalar data cache with write-through capabilities for a vector processor	711/140
72	US 57109 32 A	<input checked="" type="checkbox"/>	Parallel computer comprised of processor elements having a local memory and an enhanced data transfer mechanism	712/14
73	US 57064 88 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	712/223
74	US 56873 64 A	<input checked="" type="checkbox"/>	Method for learning to infer the topical content of documents based upon their lexical content	704/5
75	US 56779 51 A	<input checked="" type="checkbox"/>	Adaptive filter and method for implementing echo cancellation	379/406 .08
76	US 56690 13 A	<input checked="" type="checkbox"/>	System for transferring M elements X times and transferring N elements one time for an array that is X*M+N long responsive to vector type instructions	710/5
77	US 56641 34 A	<input checked="" type="checkbox"/>	Data processor for performing a comparison instruction using selective enablement and wired boolean logic	712/245
78	US 56597 66 A	<input checked="" type="checkbox"/>	Method and apparatus for inferring the topical content of a document based upon its lexical content without supervision	704/9
79	US 56045 45 A	<input checked="" type="checkbox"/>	Methods and apparatus for enhancing gray scale images	348/671
80	US 56008 46 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	712/5
81	US 55985 71 A	<input checked="" type="checkbox"/>	Data processor for conditionally modifying extension bits in response to data processing instruction execution	712/9
82	US 55926 80 A	<input checked="" type="checkbox"/>	Abnormal packet processing system	714/1
83	US 55926 28 A	<input checked="" type="checkbox"/>	Data communication system which guarantees at a transmission station the arrival of transmitted data to a receiving station and method thereof	709/200
84	US 55749 24 A	<input checked="" type="checkbox"/>	Vector processing device that utilizes post marks to ensure serialization of access requests of vector store instructions	712/7

	Document ID	U	Title	Current OR
85	US 55726 89 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	712/200
86	US 55599 73 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	712/241
87	US 55554 28 A	<input checked="" type="checkbox"/>	Activity masking with mask context of SIMD processors	712/22
88	US 55487 68 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	712/200
89	US 55375 62 A	<input checked="" type="checkbox"/>	Data processing system and method thereof	712/234
90	US 55331 78 A	<input checked="" type="checkbox"/>	Program product for displaying a line passing through a plurality of boxes	345/419
91	US 55133 66 A	<input checked="" type="checkbox"/>	Method and system for dynamically reconfiguring a register file in a vector processor	712/22
92	US 55091 36 A	<input checked="" type="checkbox"/>	Data processing system including different throughput access sources accessing main storage in same direction	711/151
93	US 54817 43 A	<input checked="" type="checkbox"/>	Minimal instruction set computer architecture and multiple instruction issue method	712/23
94	US 54816 58 A	<input checked="" type="checkbox"/>	Method and apparatus for displaying a line passing through a plurality of boxes	345/419
95	US 54758 49 A	<input checked="" type="checkbox"/>	Memory control device with vector processors and a scalar processor	712/6
96	US 54469 13 A	<input checked="" type="checkbox"/>	Method and system for nonsequential execution of intermixed scalar and vector instructions in a data processing system utilizing a finish instruction array	712/2
97	US 54308 56 A	<input checked="" type="checkbox"/>	Data processing system simultaneously performing plural translations of virtual addresses having different page sizes	711/209
98	US 54267 54 A	<input checked="" type="checkbox"/>	Cross-interrogate method and means for combined scalar and vector processing system	711/124
99	US 54086 77 A	<input checked="" type="checkbox"/>	Vector parallel computer	712/6
100	US 53197 91 A	<input checked="" type="checkbox"/>	System for predicting memory fault in vector processor by sensing indication signal to scalar processor to continue a next vector instruction issuance	712/3
101	US 53195 87 A	<input checked="" type="checkbox"/>	Computing element for neural networks	708/522
102	US 53177 17 A	<input checked="" type="checkbox"/>	Apparatus and method for main memory unit protection using access and fault logic signals	711/163
103	US 53174 77 A	<input checked="" type="checkbox"/>	High density interconnection assembly	361/683
104	US 53011 08 A	<input checked="" type="checkbox"/>	Computed tomography system with z-axis correction	378/8
105	US 52972 55 A	<input checked="" type="checkbox"/>	Parallel computer comprised of processor elements having a local memory and an enhanced data transfer mechanism	712/14
106	US 52936 26 A	<input checked="" type="checkbox"/>	Clock distribution apparatus and processes particularly useful in multiprocessor systems	713/401
107	US 52769 02 A	<input checked="" type="checkbox"/>	Memory access system for vector data processed or to be processed by a vector processor	712/6

	Document ID	U	Title	Current OR
108	US 52631 44 A	<input checked="" type="checkbox"/>	Method and apparatus for sharing data between processors in a computer system	711/121
109	US 52611 11 A	<input checked="" type="checkbox"/>	Pipelined processor for vector data classification according to vector attributes using coupled comparator chain and logic gate to respective bin chain	712/7
110	US 52573 94 A	<input checked="" type="checkbox"/>	Logical expression processing pipeline using pushdown stacks for a vector computer	712/7
111	US 52476 35 A	<input checked="" type="checkbox"/>	Vector processing system for invalidating scalar cache memory block indicated by address in tentative vector store instruction	711/3
112	US 52455 50 A	<input checked="" type="checkbox"/>	Apparatus for wire routing of VLSI	716/13
113	US 52261 71 A	<input checked="" type="checkbox"/>	Parallel vector processing system for individual and broadcast distribution of operands and control information	712/9
114	US 52187 09 A	<input checked="" type="checkbox"/>	Special purpose parallel computer architecture for real-time control and simulation in robotic applications	712/22
115	US 52147 69 A	<input checked="" type="checkbox"/>	Multiprocessor control system	711/151
116	US 52108 34 A	<input checked="" type="checkbox"/>	High speed transfer of instructions from a master to a slave processor	712/207
117	US 51971 38 A	<input checked="" type="checkbox"/>	Reporting delayed coprocessor exceptions to code threads having caused the exceptions by saving and restoring exception state during code thread switching	712/222
118	US 51796 74 A	<input checked="" type="checkbox"/>	Method and apparatus for predicting valid performance of virtual-address to physical-address translations	711/204
119	US 51703 57 A	<input checked="" type="checkbox"/>	Paper machine controller for operating slices and method of controlling the same	700/129
120	US 51685 73 A	<input checked="" type="checkbox"/>	Memory device for storing vector registers	712/4
121	US 51135 21 A	<input checked="" type="checkbox"/>	Method and apparatus for handling faults of vector instructions causing memory management exceptions	714/15
122	US 50739 70 A	<input checked="" type="checkbox"/>	Vector processing apparatus allowing succeeding vector instruction chain processing upon completion of decoding of a preceding vector instruction chain	712/7
123	US 50438 86 A	<input checked="" type="checkbox"/>	Load/store with write-intent for write-back caches	711/143
124	US 50383 12 A	<input checked="" type="checkbox"/>	Data processing system capable of performing vector/matrix processing and arithmetic processing unit incorporated therein	708/520
125	US 50291 23 A	<input checked="" type="checkbox"/>	Information processing device capable of indicating performance	708/670
126	US 50070 05 A	<input checked="" type="checkbox"/>	Data processing system	345/473
127	US 50016 27 A	<input checked="" type="checkbox"/>	Multiprocessor control system for selectively executing vector instructions from scaler units to be executed in a vector unit	712/229
128	US 49808 17 A	<input checked="" type="checkbox"/>	Vector register system for executing plural read/write commands concurrently and independently routing data to plural read/write ports	712/4
129	US 49741 98 A	<input checked="" type="checkbox"/>	Vector processing system utilizing firm ware control to prevent delays during processing operations	712/8
130	US 49741 45 A	<input checked="" type="checkbox"/>	Processor system including a paging processor for controlling paging between a main storage and an extended storage	712/6

	Document ID	U	Title	Current OR
131	US 49640 35 A	<input checked="" type="checkbox"/>	Vector processor capable of high-speed access to processing results from scalar processor	712/3
132	US 49492 92 A	<input checked="" type="checkbox"/>	Vector processor for processing recurrent equations at a high speed	708/520
133	US 49454 79 A	<input checked="" type="checkbox"/>	Tightly coupled scientific processing system	712/3
134	US 49425 18 A	<input checked="" type="checkbox"/>	Cache store bypass for computer	711/138
135	US 49362 77 A	<input checked="" type="checkbox"/>	System for monitoring and/or controlling multiple cylinder engine performance	123/436
136	US 49282 38 A	<input checked="" type="checkbox"/>	Scalar data arithmetic control system for vector arithmetic processor	712/7
137	US 49263 17 A	<input checked="" type="checkbox"/>	Hierarchical memory system with logical cache, physical cache, and address translation unit for generating a sequence of physical addresses	711/3
138	US 48751 61 A	<input checked="" type="checkbox"/>	Scientific processor vector file organization	711/157
139	US 48736 29 A	<input checked="" type="checkbox"/>	Instruction processing unit for computer	712/213
140	US 48581 15 A	<input checked="" type="checkbox"/>	Loop control mechanism for scientific processor	712/7
141	US 48498 82 A'	<input checked="" type="checkbox"/>	Vector processing system for processing plural vector instruction streams	712/6
142	US 48414 38 A	<input checked="" type="checkbox"/>	System for generating mask pattern for vector data processor	712/5
143	US 48356 72 A	<input checked="" type="checkbox"/>	Access lock apparatus for use with a high performance storage unit of a digital data processing system	711/151
144	US 48274 07 A	<input checked="" type="checkbox"/>	Vector processing system	712/6
145	US 48211 81 A	<input checked="" type="checkbox"/>	Method for converting a source program of high level language statement into an object program for a vector processor	717/106
146	US 48129 72 A	<input checked="" type="checkbox"/>	Microcode computer having dispatch and main control stores for storing the first and the remaining microinstructions of machine instructions	712/211
147	US 48036 20 A	<input checked="" type="checkbox"/>	Multi-processor system responsive to pause and pause clearing instructions for instruction execution control	712/203
148	US 47915 60 A	<input checked="" type="checkbox"/>	Macro level control of an activity switch in a scientific vector processor which processor requires an external executive control program	712/242
149	US 47915 59 A	<input checked="" type="checkbox"/>	High-speed instruction control for vector processors with remapping	712/213
150	US 47899 25 A	<input checked="" type="checkbox"/>	Vector data logical usage conflict detection	712/7
151	US 47775 93 A	<input checked="" type="checkbox"/>	Vector processing apparatus including means for identifying the occurrence of exceptions in the processing of vector elements	712/9
152	US 47713 80 A	<input checked="" type="checkbox"/>	Virtual vector registers for vector processing system	712/6
153	US 47697 70 A	<input checked="" type="checkbox"/>	Address conversion for a multiprocessor system having scalar and vector processors	711/206

	Document ID	U	Title	Current OR
154	US 47681 46 A	<input checked="" type="checkbox"/>	Vector data refer circuit with a preceding paging control for a vector processor apparatus therefor	711/207
155	US 47605 25 A	<input checked="" type="checkbox"/>	Complex arithmetic vector processor for performing control function, scalar operation, and set-up of vector signal processing instruction	712/2
156	US 47574 40 A	<input checked="" type="checkbox"/>	Pipelined data stack with access through-checking	714/53
157	US 47220 52 A	<input checked="" type="checkbox"/>	Multiple unit adapter	710/305
158	US 47220 49 A	<input checked="" type="checkbox"/>	Apparatus for out-of-order program execution	712/3
159	US 47061 91 A	<input checked="" type="checkbox"/>	Local store for scientific vector processor	712/3
160	US 46972 33 A	<input checked="" type="checkbox"/>	Partial duplication of pipelined stack with data integrity checking	711/169
161	US 46850 76 A	<input checked="" type="checkbox"/>	Vector processor for processing one vector instruction with a plurality of vector processing units	708/520
162	US 46807 30 A	<input checked="" type="checkbox"/>	Storage control apparatus	711/169
163	US 46740 32 A	<input checked="" type="checkbox"/>	High-performance pipelined stack with over-write protection	711/169
164	US 46494 75 A	<input checked="" type="checkbox"/>	Multiple port memory with port decode error detector	711/149
165	US 46462 33 A	<input checked="" type="checkbox"/>	Physical cache unit for computer	711/3
166	US 46334 34 A	<input checked="" type="checkbox"/>	High performance storage unit	713/400
167	US 46202 75 A	<input checked="" type="checkbox"/>	Computer system	712/6
168	US 46009 86 A	<input checked="" type="checkbox"/>	Pipelined split stack with high performance interleaved decode	711/169
169	US 45946 82 A	<input checked="" type="checkbox"/>	Vector processing	712/6
170	US 45573 86 A	<input checked="" type="checkbox"/>	System to measure geometric and electromagnetic characteristics of objects	209/556
171	US 43542 49 A	<input checked="" type="checkbox"/>	Processing unit for multiplying two mathematical quantities including at least one complex multiplier	708/622
172	US 43531 19 A	<input checked="" type="checkbox"/>	Adaptive antenna array including batch covariance relaxation apparatus and method	702/194
173	US 41019 60 A	<input type="checkbox"/>	Scientific processor	712/22

	L #	Hits	Search Text	DBs
1	L1	396	(shar\$3 common unified united combin\$3 mode) near20 (scalar near10 (vector pack\$3 simd))	USPAT; US-PGPUB
2	L2	9791	(tag bit field flag indicat\$3 identif\$6) near30 ((activ\$5 valid\$4 enabl\$3 disabl\$3 invalid\$4 set\$4) near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	USPAT; US-PGPUB
3	L3	72	1 and 2	USPAT; US-PGPUB
4	L5	1285	(tag bit field flag indicat\$3 identif\$6) near30 ((activ\$5 valid\$4 enabl\$3 disabl\$3 invalid\$4 set\$4) near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	EPO; JPO; DERWENT; IBM TDB
5	L6	0	4 and 5	EPO; JPO; DERWENT; IBM TDB
6	L4	74	(shar\$3 common unified united combin\$3 mode) near20 (scalar near10 (vector pack\$3 simd))	EPO; JPO; DERWENT; IBM TDB
7	L9	34	2 near30 scalar	USPAT; US-PGPUB
8	L10	1	5 near30 scalar	EPO; JPO; DERWENT; IBM TDB
9	L11	47858	(tag bit field flag indicat\$3 identif\$6) near10 ((data datum subdata portion part\$3 section segment sub) near10 register)	USPAT; US-PGPUB
10	L12	290	11 near30 ((activ\$5 valid\$4 enabl\$3 disabl\$3 invalid\$4 set\$4) near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	USPAT; US-PGPUB
11	L13	22	12 and (scalar near20 (vector pack\$3 simd))	USPAT; US-PGPUB
12	L16	15045	(tag bit field flag indicat\$3 identif\$6) near10 ((data datum subdata portion part\$3 section segment sub) near10 register)	EPO; JPO; DERWENT; IBM TDB
13	L17	33	16 near30 ((activ\$5 valid\$4 enabl\$3 disabl\$3 invalid\$4 set\$4) near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	EPO; JPO; DERWENT; IBM TDB
14	L18	0	17 and (scalar near20 (vector pack\$3 simd))	EPO; JPO; DERWENT; IBM TDB
15	L19	145	1 and ((activ\$5 valid\$4 enabl\$3 disabl\$3 invalid\$4 set\$4) near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	USPAT; US-PGPUB
16	L20	73	19 not (3 13)	USPAT; US-PGPUB
17	L21	39	1 near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block))	USPAT; US-PGPUB
18	L24	89	(scalar near10 (vector SIMD packed)) near20 (alu (datapath (data adj1 path)) ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	EPO; JPO; DERWENT; IBM TDB
19	L22	371	(scalar near10 (vector SIMD packed)) near20 (alu (datapath (data adj1 path)) ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	USPAT; US-PGPUB
20	L26	198	(scalar near10 (vector SIMD packed)) near20 (alu (datapath (data adj1 path)) ((function\$3 operation\$3) adj2 (unit module block)))	USPAT; US-PGPUB
21	L27	173	22 not 26	USPAT; US-PGPUB

	L #	Hits	Search Text	DBs
1	L1	396	(shar\$3 common unified united combin\$3 mode) near20 (scalar near10 (vector pack\$3 simd))	USPAT; US-PGPUB
2	L2	9791	(tag bit field flag indicat\$3 identif\$6) near30 ((activ\$5 valid\$4 enabl\$3 disabl\$3 invalid\$4 set\$4) near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	USPAT; US-PGPUB
3	L3	72	1 and 2	USPAT; US-PGPUB
4	L5	1285	(tag bit field flag indicat\$3 identif\$6) near30 ((activ\$5 valid\$4 enabl\$3 disabl\$3 invalid\$4 set\$4) near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	EPO; JPO; DERWENT; IBM_TDB
5	L6	0	4 and 5	EPO; JPO; DERWENT; IBM_TDB
6	L4	74	(shar\$3 common unified united combin\$3 mode) near20 (scalar near10 (vector pack\$3 simd))	EPO; JPO; DERWENT; IBM_TDB
7	L7	9719	2 not 3	USPAT; US-PGPUB
8	L8	72	2 not 7	USPAT; US-PGPUB
9	L9	34	2 near30 scalar	USPAT; US-PGPUB
10	L10	1	5 near30 scalar	EPO; JPO; DERWENT; IBM_TDB

	L #	Hits	Search Text	DBs
1	L1	396	(shar\$3 common unified united combin\$3 mode) near20 (scalar near10 (vector pack\$3 simd))	USPAT; US_PGPUB
2	L2	9791	(tag bit field flag indicat\$3 identif\$6) near30 ((activ\$5 valid\$4 enabl\$3 disabl\$3 invalid\$4 set\$4) near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	USPAT; US_PGPUB
3	L3	72	1 and 2	USPAT; US_PGPUB
4	L5	1285	(tag bit field flag indicat\$3 identif\$6) near30 ((activ\$5 valid\$4 enabl\$3 disabl\$3 invalid\$4 set\$4) near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	EPO; JPO; DERWENT; IBM_TDB
5	L6	0	4 and 5	EPO; JPO; DERWENT; IBM_TDB
6	L4	74	(shar\$3 common unified united combin\$3 mode) near20 (scalar near10 (vector pack\$3 simd))	EPO; JPO; DERWENT; IBM_TDB
7	L9	34	2 near30 scalar	USPAT; US_PGPUB
8	L10	1	5 near30 scalar	EPO; JPO; DERWENT; IBM_TDB
9	L11	47858	(tag bit field flag indicat\$3 identif\$6) near10 ((data datum subdata portion part\$3 section segment sub) near10 register)	USPAT; US_PGPUB
10	L12	290	11 near30 ((activ\$5 valid\$4 enabl\$3 disabl\$3 invalid\$4 set\$4) near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	USPAT; US_PGPUB
11	L13	22	12 and (scalar near20 (vector pack\$3 simd))	USPAT; US_PGPUB
12	L16	15045	(tag bit field flag indicat\$3 identif\$6) near10 ((data datum subdata portion part\$3 section segment sub) near10 register)	EPO; JPO; DERWENT; IBM_TDB
13	L17	33	16 near30 ((activ\$5 valid\$4 enabl\$3 disabl\$3 invalid\$4 set\$4) near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	EPO; JPO; DERWENT; IBM_TDB
14	L18	0	17 and (scalar near20 (vector pack\$3 simd))	EPO; JPO; DERWENT; IBM_TDB

	Docum ent ID	U	Title	Current OR
1	JP 10187 661 A	<input type="checkbox"/>	METHOD FOR ENTERING SCALAR VALUE OF COMPUTER INTO VECTOR	
2	JP 09198 374 A	<input checked="" type="checkbox"/>	VECTOR PROCESSOR	
3	JP 09091 142 A	<input checked="" type="checkbox"/>	PARALLEL COMPUTER SYSTEM	
4	JP 09062 655 A	<input checked="" type="checkbox"/>	MULTIPROCESSOR SYSTEM	
5	JP 08050 575 A	<input checked="" type="checkbox"/>	PROGRAMMABLE PROCESSOR, METHOD FOR PERFORMING DIGITAL SIGNAL PROCESSING BY USING THE PROGRAMMABLE PROCESSOR AND ITS IMPROVEMENT	
6	JP 07028 761 A	<input checked="" type="checkbox"/>	ASYMMETRICAL VECTOR MULTIPROCESSOR	
7	JP 06168 263 A	<input checked="" type="checkbox"/>	VECTOR PROCESSOR	
8	JP 05197 743 A	<input checked="" type="checkbox"/>	VECTOR PROCESSOR	
9	JP 03184 127 A	<input checked="" type="checkbox"/>	REGISTER SAVING CONTROL METHOD	
10	JP 03077 141 A	<input checked="" type="checkbox"/>	DIVISION PROCESSING SYSTEM FOR VECTOR OPERATION TRAIN	
11	JP 02297 624 A	<input checked="" type="checkbox"/>	SYSTEM FOR COMPARING AND COMPUTING SIZE OF VECTOR	
12	JP 02253 471 A	<input checked="" type="checkbox"/>	CENTRAL PROCESSING UNIT	
13	JP 02148 260 A	<input checked="" type="checkbox"/>	PARALLEL EXECUTION SYSTEM	
14	JP 02077 968 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR	
15	JP 02015 369 A	<input checked="" type="checkbox"/>	METHOD FOR EXECUTING INSTRUCTION OF VECTOR PROCESSING SYSTEM AND DEVICE THEREFOR	
16	JP 01318 161 A	<input checked="" type="checkbox"/>	VECTOR PROCESSOR	
17	JP 01222 376 A	<input checked="" type="checkbox"/>	BUFFER STORAGE DEVICE	
18	JP 01222 375 A	<input checked="" type="checkbox"/>	BUFFER STORAGE DEVICE	
19	JP 01213 721 A	<input checked="" type="checkbox"/>	COMPILER SYSTEM	
20	JP 61187 076 A	<input checked="" type="checkbox"/>	VECTOR PROCESSOR	
21	JP 61131 169 A	<input checked="" type="checkbox"/>	MULTI-PROCESSOR SYSTEM	
22	JP 61095 477 A	<input checked="" type="checkbox"/>	VECTOR PROCESSING DEVICE	
23	JP 61011 880 A	<input checked="" type="checkbox"/>	VECTOR PROCESSOR	

	Document ID	U	Title	Current OR
24	JP 60140 441 A	<input checked="" type="checkbox"/>	LOGICAL SIMULATION PROCESSING UNIT	
25	JP 60134 945 A	<input checked="" type="checkbox"/>	DATA BASE PROCESSING SYSTEM	
26	JP 58134 357 A	<input checked="" type="checkbox"/>	ARRAY PROCESSOR	
27	JP 58046 467 A	<input checked="" type="checkbox"/>	VECTOR PROCESSOR	
28	JP 57157 373 A	<input checked="" type="checkbox"/>	VECTOR PROCESSOR	
29	JP 57109 084 A	<input checked="" type="checkbox"/>	SCHEDULE SYSTEM FOR INSTRUCTION IN PARALLEL COMPUTER HAVING PLURAL OPERATING DEVICES	
30	WO 31006 02 A2	<input checked="" type="checkbox"/>	A SCALAR/VECTOR PROCESSOR	
31	WO 20671 37 A1	<input checked="" type="checkbox"/>	VECTOR AND SCALAR SIGNAL PROCESSING	
32	EP 68123 6 A1	<input checked="" type="checkbox"/>	Space vector data path.	
33	EP 60798 8 A1	<input checked="" type="checkbox"/>	Program controlled processor.	
34	EP 60058 3 A1	<input checked="" type="checkbox"/>	Vector processing device.	
35	EP 16706 1 A2	<input checked="" type="checkbox"/>	Vector processing computer.	
36	EP 10512 5 A2	<input checked="" type="checkbox"/>	Data processing system.	
37	GB 23904 43 A	<input checked="" type="checkbox"/>	Microprocessor core with scalar and vector units for e.g. graphics processor, has execution unit and two sets of registers, with one register set not accessible to compiler-generated code but exclusively available to applications program	
38	WO 20031 00602 A	<input checked="" type="checkbox"/>	Scalar/vector processor for mobile communication system, has vector and scalar sections of functional units co-operating by scalar section arranged to provide and/or consume scalar required by and/or supplied by vector section	
39	US 65913 45 B	<input checked="" type="checkbox"/>	Processor for computer systems, has vector execution unit that connects to scalar processor unit to transfer data and instructions and retrieves strided vectors of data and instructions that are stored in cache memory	
40	GB 23828 87 A	<input checked="" type="checkbox"/>	Processor for image processing has instruction decoder directing instructions to scalar and vector processing units	
41	GB 23826 73 A	<input checked="" type="checkbox"/>	Vector processing system for executing vector instructions defining pair of values in multimedia applications uses plural parallel processing unit to process instructions	
42	US 20030 03722 1 A	<input checked="" type="checkbox"/>	Microprocessor performs single vector operation on several data elements in parallel, and scalar operation on data element, during respective vector and scalar operation modes	
43	JP 20022 97566 A	<input checked="" type="checkbox"/>	Vector processing command passing circuit for vector processing apparatus, transmits held vector processing command to memory access request generating circuit, when load command is received	

	Document ID	U	Title	Current OR
44	US 20020 13087 4 A	<input checked="" type="checkbox"/>	Graphics processing method in 3D graphics system, involves expanding instructions to derive sequence of scalar operations, and pipelining execution of derived scalar operations	
45	RU 21768 15 C	<input checked="" type="checkbox"/>	Digital information processing device	
46	EP 10110 52 A	<input checked="" type="checkbox"/>	Processing system with shared memory type vector to run applications with vector and scalar resources by setting central processing units (CPU) as master scalar processing unit accompanied by slave operating multi-vector pipeline units	
47	US 63016 53 B	<input checked="" type="checkbox"/>	Digital signal processor for use in executing multiple instructions, has coupling fabric which writes and reads information from N storage elements and M data path units	
48	US 59266 43 A	<input checked="" type="checkbox"/>	Data driven processor for performing parallel scalar and vector processing	
49	US 59130 69 A	<input checked="" type="checkbox"/>	Distributed vector processing system for scalar or vector multiprocessor computer system	
50	JP 10207 720 A	<input checked="" type="checkbox"/>	Information processor with provision for operating in scalar and vector modes - has controller that switches operational mode to scalar and vector modes during which scalar and vector instructions are executed using pair of register sets as scalar and vector register sets	
51	US 57428 42 A	<input checked="" type="checkbox"/>	Processor for executing scalar or vector operations - includes execution unit which executes vector and scalar operations in parallel and executes command, causing selected operation to be executed, in command store in pipelined process	
52	US 58058 75 A	<input checked="" type="checkbox"/>	Vector processing system with multi-operation run-time configurable pipelines - controls configuration of vector functional unit's pipelines with value held in scalar register named by vector instruction	
53	US 56597 06 A	<input checked="" type="checkbox"/>	Instruction control mechanism for scalar-vector processor in multiprocessor system - beginning filling of first part of instruction cache with first instruction simultaneous to previously begun fill operation to fill instruction cache with fifth instruction	
54	JP 09091 142 A	<input checked="" type="checkbox"/>	Parallel computer system - has vector and scalar processor elements of mxn dimension, having loose or tight coupling	
55	US 55443 37 A	<input checked="" type="checkbox"/>	Data processor for scalar and vector processing - includes vector registers and functional units with unit responding to instructions to initiate vector processing with vector registers maintaining busy status	
56	US 55308 81 A	<input checked="" type="checkbox"/>	Vector processor system for instruction set architecture corresponding to mingled-type-and-separate-type-programs - has vector processing unit connected to two scalar processing unit and memory storage	
57	JP 08153 088 A	<input checked="" type="checkbox"/>	Vector data calculation method for data-processor with vector unit - involves computing vector data, e.g. factor of vector, according to estimated execution time of scalar instruction	
58	EP 68123 6 A	<input checked="" type="checkbox"/>	Programmable processor for space vector data path to integrate SIMD into general purpose programmable processor - specifies whether each instruction is in either vector or scalar mode and sends signal to processing unit	
59	US 54267 54 A	<input checked="" type="checkbox"/>	Combined scalar and vector processing system - has scalar XI directory recording lines currently being stored by scalar processors, and vector store registers recording lines currently being stored into by vector processors	
60	US 54230 51 A	<input checked="" type="checkbox"/>	CPU for integrating vector and scalar operations - has vector operation execution unit designed to support scalar processing by pipelining fixed and float point instructions functional units included in it	

	Document ID	U	Title	Current OR
61	US 54189 73 A	<input checked="" type="checkbox"/>	Digital computer system with cache controller coordinating both vector and scalar operations - has cache controller which includes vector logic which is responsive to vector information written in intra-processor registers by execution unit	
62	EP 64687 7 A	<input checked="" type="checkbox"/>	Scalar computer with vector data processing facility - has multi-element vector registers controlled to sequence transfer of vector data between main memory and processing unit of scalar computer sequentially	
63	EP 60058 3 A	<input checked="" type="checkbox"/>	Vector processing unit for large quantity of vector data using one instruction - performs information transfer in accordance with serialising process among access requests by using post instruction and wait instruction with sandwiched access instruction serially carried out	
64	US 52611 11 A	<input checked="" type="checkbox"/>	Pipeline processing unit for computer nuclear simulation - has pipelines for classifying data by attributes and data expressed by logical values, decision pipeline for detecting contradiction in data attributes and address preset processing unit for previously computing variable address by parallel	
65	US 35269 E	<input checked="" type="checkbox"/>	Portable computer protective reflex system - monitors output of three axis accelerometer and passes high priority interrupt to central processor unit in event of acceleration event within preset range of values	
66	US 51230 95 A	<input checked="" type="checkbox"/>	Data processing system including integrated scalar and vector - addresses vector by scalar processor providing virtual-to-physical memory translation for both operations	
67	SU 17288 61 A	<input checked="" type="checkbox"/>	Real numbers scalar and vector operations calculator - has non-equivalence gate at sign forming input of corresp. operational element	
68	EP 42832 6 A	<input checked="" type="checkbox"/>	Processor array system with an SIMD architecture - comprises single bit processor elements with cyclic data path unidirectional shift register and arithmetic unit	
69	US 49910 83 A	<input checked="" type="checkbox"/>	Extending address space of vector processor - changing interruption processing routine or adding sub-routine without changing main part of operating system regarding paging	
70	US 49741 45 A	<input checked="" type="checkbox"/>	Processor system including paging processor for controlling paging - has storage control unit store access request, and circuit operative in response to interrupt vector access request	
71	EP 39863 9 A	<input checked="" type="checkbox"/>	Serialised system between vector instruction and scalar instruction - has scalar unit receive scalar and vector instructions to perform scalar processing and transfer to vector unit	
72	EP 39689 2 A	<input checked="" type="checkbox"/>	Data processing appts. nulling scalar cache memory - according to vector store instruction via instruction passing issuing control before vector store instruction	
73	US 49454 79 A	<input checked="" type="checkbox"/>	Tightly coupled data processing system - has scientific processor-coupled-to-host-processors-through-common-access-to-virtual address space in high speed storage	
74	EP 45467 1 B	<input checked="" type="checkbox"/>	Computer look-ahead control logic for instruction issue - checks for resource conflicts before the instruction issues by comparing with instructions ahead	
75	EP 36819 3 A	<input checked="" type="checkbox"/>	Information processing device cable of indicating performance - has periodic signal sequence generator and device to successively count floating point operation elements	
76	US 49263 17 A	<input checked="" type="checkbox"/>	Hierarchical computer memory with logical and physical caches - has address translation unit for generating sequence of physical addresses for high speed vector and scalar processing	
77	EP 35919 2 A	<input checked="" type="checkbox"/>	Vector register control for more efficient computer operation - using memory modules identified by new address number produced by combining address number and scalar unit number	
78	EP 33551 4 A	<input checked="" type="checkbox"/>	Data processor for executing both scalar and vector instructions - allows scalar instruction execution in presence of arithmetic exception condition in vector processor unit	
79	EP 33336 6 A	<input checked="" type="checkbox"/>	Multi-tasking data processing system - stores vector state information at locations corresponding to last vector-using process when it differs from current process	

	Document ID	U	Title	Current OR
80	EP 33336 5 A	<input checked="" type="checkbox"/>	System for handling memory management exceptions - halts execution of faulting vector instruction and continues scalar instruction execution with subsequent resumption of vector instruction	
81	EP 34849 5 B	<input checked="" type="checkbox"/>	Main memory and cache system for vector and scalar processors - provides efficient use of cache by vector processor by pre-loading vector data blocks into cache memory	
82	US 48377 30 A	<input checked="" type="checkbox"/>	Digital computer performing vector and scalar operations - links scalar results directly to scalar operation inputs on bidirectional databus	
83	US 47605 25 A	<input checked="" type="checkbox"/>	Complex arithmetic vector processor module - performs control function scalar operation and set-up of vector signal processing instruction at high speed	
84	EP 23597 7 A	<input checked="" type="checkbox"/>	Bi-directional databus system supporting vector-scaler superposition - has three-sets of bidirectional memory databases for transfer between main memory and buffer units	
85	DE 36385 72 A	<input checked="" type="checkbox"/>	High speed vector processor - has scalar instruction decoder coupled to indicator register to control operation of vector and scalar cycles	
86	EP 21161 7 A	<input checked="" type="checkbox"/>	Scientific processor for data processing system - has scalar and vector processor modules operable under program control of one or more host processors	
87	EP 11430 4 A	<input checked="" type="checkbox"/>	Vector processing hardware assist appts. - is for digital processor using cache memory to have vector operand elements read from it and operation results written into it	
88	EP 10512 5 A	<input checked="" type="checkbox"/>	Data processing system - has two scalar processing units to match high speed processing capabilities of single vector processor	
89	EP 85435 A	<input type="checkbox"/>	Array processor comprised of vector processors using vector registers - has vector registers and pipe-line control through which double-do-loop processings are executed in parallel	

	Document ID	U	Title	Current OR
1	US 20040 01974 7 A1	<input type="checkbox"/>	Narrow/wide cache	711/141
2	US 20040 01568 2 A1	<input checked="" type="checkbox"/>	Application registers	712/228
3	US 20040 01567 7 A1	<input checked="" type="checkbox"/>	Digital signal processor with SIMD organization and flexible data manipulation	712/22
4	US 20030 16366 7 A1	<input checked="" type="checkbox"/>	Vector processing system	712/7
5	US 20030 15902 3 A1	<input checked="" type="checkbox"/>	Repeated instruction execution	712/241
6	US 20030 15901 7 A1	<input checked="" type="checkbox"/>	Data access in a processor	712/34
7	US 20030 15901 6 A1	<input checked="" type="checkbox"/>	Data access in a processor	712/4
8	US 20030 15436 1 A1	<input checked="" type="checkbox"/>	Instruction execution in a processor	712/214
9	US 20030 03722 1 A1	<input checked="" type="checkbox"/>	Processor implementation having unified scalar and SIMD datapath	712/3
10	US 20030 01867 6 A1	<input checked="" type="checkbox"/>	Multi-function floating point arithmetic pipeline	708/501
11	US 66292 31 B1	<input checked="" type="checkbox"/>	System and method for efficient register file conversion of denormal numbers between scalar and SIMD formats	712/1
12	US 64003 06 B1	<input checked="" type="checkbox"/>	Multi-channel moving target radar detection and imaging apparatus and method	342/25
13	US 62667 59 B1	<input checked="" type="checkbox"/>	Register scoreboard to support overlapped execution of vector memory reference instructions in a vector processor	712/5
14	US 59464 96 A	<input checked="" type="checkbox"/>	Distributed vector architecture	712/2
15	US 59130 69 A	<input checked="" type="checkbox"/>	Interleaving memory in distributed vector architecture multiprocessor system	712/2
16	US 57782 41 A	<input checked="" type="checkbox"/>	Space vector data path	712/20
17	US 57457 21 A	<input checked="" type="checkbox"/>	Partitioned addressing apparatus for vector/scalar registers	712/208
18	US 57178 81 A	<input checked="" type="checkbox"/>	Data processing system for processing one and two parcel instructions	712/205
19	US 57064 90 A	<input checked="" type="checkbox"/>	Method of processing conditional branch instructions in scalar/vector processor	712/234

	Document ID	U	Title	Current OR
20	US 56690 13 A	<input checked="" type="checkbox"/>	System for transferring M elements X times and transferring N elements one time for an array that is X*M+N long responsive to vector type instructions	710/5
21	US 56597 06 A	<input checked="" type="checkbox"/>	Vector/scalar processor with simultaneous processing and instruction cache filling	711/125
22	US 56405 24 A	<input checked="" type="checkbox"/>	Method and apparatus for chaining vector instructions	712/222
23	US 56236 50 A	<input checked="" type="checkbox"/>	Method of processing a sequence of conditional vector IF statements	712/234
24	US 55985 47 A	<input checked="" type="checkbox"/>	Vector processor having functional unit paths of differing pipeline lengths	712/222
25	US 55617 84 A	<input checked="" type="checkbox"/>	Interleaved memory access system having variable-sized segments logical address spaces and means for dividing/mapping physical address into higher and lower order addresses	711/157
26	US 55443 37 A	<input checked="" type="checkbox"/>	Vector processor having registers for control by vector resistors	712/4
27	US 55376 06 A	<input checked="" type="checkbox"/>	Scalar pipeline replication for parallel vector element processing	712/7
28	US 55176 66 A	<input checked="" type="checkbox"/>	Program controlled processor wherein vector distributor and vector coupler operate independently of sequencer	712/3
29	US 54469 13 A	<input checked="" type="checkbox"/>	Method and system for nonsequential execution of intermixed scalar and vector instructions in a data processing system utilizing a finish instruction array	712/2
30	US 54308 84 A	<input checked="" type="checkbox"/>	Scalar/vector processor	712/3
31	US 53903 29 A	<input checked="" type="checkbox"/>	Responding to service requests using minimal system-side context in a multiprocessor environment	718/108
32	US 53597 18 A	<input checked="" type="checkbox"/>	Early scalable instruction set machine alu status prediction apparatus	712/221
33	US 53414 82 A	<input checked="" type="checkbox"/>	Method for synchronization of arithmetic exceptions in central processing units having pipelined execution units simultaneously executing instructions	712/244
34	US 53074 78 A	<input checked="" type="checkbox"/>	Method for inserting a path instruction during compilation of computer programs for processors having multiple functional units	703/22
35	US 52993 19 A	<input checked="" type="checkbox"/>	High performance interlock collapsing SCISM ALU apparatus	712/221
36	US 52915 81 A	<input checked="" type="checkbox"/>	Apparatus and method for synchronization of access to main memory signal groups in a multiprocessor data processing system	711/152
37	US 52788 40 A	<input checked="" type="checkbox"/>	Apparatus and method for data induced condition signalling	714/25
38	US 52769 02 A	<input checked="" type="checkbox"/>	Memory access system for vector data processed or to be processed by a vector processor	712/6
39	US 52611 13 A	<input checked="" type="checkbox"/>	Apparatus and method for single operand register array for vector and scalar data processing operations	712/8
40	US 52187 12 A	<input checked="" type="checkbox"/>	Providing a data processor with a user-mode accessible mode of operations in which the processor performs processing operations without interruption	710/261
41	US 52029 75 A	<input checked="" type="checkbox"/>	Method for optimizing instruction scheduling for a processor having multiple functional resources	717/151

	Document ID	U	Title	Current OR
42	US 51971 30 A	<input checked="" type="checkbox"/>	Cluster architecture for a highly parallel scalar/vector multiprocessor system	712/3
43	US 51485 44 A	<input checked="" type="checkbox"/>	Apparatus and method for control of asynchronous program interrupt events in a data processing system	710/261
44	US 50634 97 A	<input checked="" type="checkbox"/>	Apparatus and method for recovering from missing page faults in vector data processing operations	712/6
45	US 50383 12 A	<input checked="" type="checkbox"/>	Data processing system capable of performing vector/matrix processing and arithmetic processing unit incorporated therein	708/520
46	US 50291 23 A	<input checked="" type="checkbox"/>	Information processing device capable of indicating performance	708/670
47	US 48377 30 A	<input checked="" type="checkbox"/>	Linking scalar results directly to scalar operation inputs on a bidirectional databus in a computer which superpositions vector and scalar operations	712/7
48	US 48036 20 A	<input checked="" type="checkbox"/>	Multi-processor system responsive to pause and pause clearing instructions for instruction execution control	712/203
49	US 47776 15 A	<input checked="" type="checkbox"/>	Backplane structure for a computer superpositioning scalar and vector operations	710/300
50	US 47605 18 A	<input checked="" type="checkbox"/>	Bi-directional databus system for supporting superposition of vector and scalar operations in a computer	710/107
51	US 46850 76 A	<input checked="" type="checkbox"/>	Vector processor for processing one vector instruction with a plurality of vector processing units	708/520
52	US 46333 89 A	<input checked="" type="checkbox"/>	Vector processor system comprised of plural vector processors	712/4
53	US 45410 46 A	<input type="checkbox"/>	Data processing system including scalar data processor and vector data processor	712/3

	L #	Hits	Search Text	DBs
1	L1	396	(shar\$3 common unified united combin\$3 mode) near20 (scalar near10 (vector pack\$3 simd))	USPAT; US_PGPUB
2	L2	9791	(tag bit field flag indicat\$3 identif\$6) near30 ((activ\$5 valid\$4 enabl\$3 disabl\$3 invalid\$4 set\$4) near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	USPAT; US_PGPUB
3	L3	72	1 and 2	USPAT; US_PGPUB
4	L5	1285	(tag bit field flag indicat\$3 identif\$6) near30 ((activ\$5 valid\$4 enabl\$3 disabl\$3 invalid\$4 set\$4) near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	EPO; JPO; DERWENT; IBM_TDB
5	L6	0	4 and 5	EPO; JPO; DERWENT; IBM_TDB
6	L4	74	(shar\$3 common unified united combin\$3 mode) near20 (scalar near10 (vector pack\$3 simd))	EPO; JPO; DERWENT; IBM_TDB
7	L9	34	2 near30 scalar	USPAT; US_PGPUB
8	L10	1	5 near30 scalar	EPO; JPO; DERWENT; IBM_TDB
9	L11	47858	(tag bit field flag indicat\$3 identif\$6) near10 ((data datum subdata portion part\$3 section segment sub) near10 register)	USPAT; US_PGPUB
10	L12	290	11 near30 ((activ\$5 valid\$4 enabl\$3 disabl\$3 invalid\$4 set\$4) near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	USPAT; US_PGPUB
11	L13	22	12 and (scalar near20 (vector pack\$3 simd))	USPAT; US_PGPUB
12	L16	15045	(tag bit field flag indicat\$3 identif\$6) near10 ((data datum subdata portion part\$3 section segment sub) near10 register)	EPO; JPO; DERWENT; IBM_TDB
13	L17	33	16 near30 ((activ\$5 valid\$4 enabl\$3 disabl\$3 invalid\$4 set\$4) near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	EPO; JPO; DERWENT; IBM_TDB
14	L18	0	17 and (scalar near20 (vector pack\$3 simd))	EPO; JPO; DERWENT; IBM_TDB
15	L19	145	1 and ((activ\$5 valid\$4 enabl\$3 disabl\$3 invalid\$4 set\$4) near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	USPAT; US_PGPUB
16	L20	73	19 not (3 13)	USPAT; US_PGPUB
17	L21	39	1 near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block))	USPAT; US_PGPUB
18	L24	89	(scalar near10 (vector simd packed)) near20 (alu (datapath (data adj1 path)) ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	EPO; JPO; DERWENT; IBM_TDB
19	L22	371	(scalar near10 (vector simd packed)) near20 (alu (datapath (data adj1 path)) ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	USPAT; US_PGPUB
20	L26	198	(scalar near10 (vector simd packed)) near20 (alu (datapath (data adj1 path)) ((function\$3 operation\$3 adj2 (unit module block)))	USPAT; US_PGPUB
21	L35	154	26 not 19	USPAT; US_PGPUB
22	L37	4364	((sav\$3 reduc\$4 lower\$3) nea10 (energy power)) and (scalar near20 (vector simd packed))	USPAT; US_PGPUB
23	L38	696	37 and ((activ\$5 valid\$4 enabl\$3 disabl\$3 invalid\$4 set\$4) near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	USPAT; US_PGPUB

	Document ID	U	Title	Current OR
1	JP 20030 99420 A	<input type="checkbox"/>	SHARED MEMORY TYPE VECTOR PROCESSING SYSTEM, ITS CONTROL METHOD AND STORAGE MEDIUM FOR STORING THE CONTROL PROGRAM OF VECTOR PROCESSING	
2	JP 20011 95390 A	<input checked="" type="checkbox"/>	OPERAND CACHE FOR VECTOR PROCESSOR	
3	JP 11272 874 A	<input checked="" type="checkbox"/>	ELECTRONIC DEVICE	
4	JP 10207 720 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR	
5	JP 09282 308 A	<input checked="" type="checkbox"/>	VECTOR INSTRUCTION CONTROL SYSTEM	
6	JP 09091 142 A	<input checked="" type="checkbox"/>	PARALLEL COMPUTER SYSTEM	
7	JP 08050 575 A	<input checked="" type="checkbox"/>	PROGRAMMABLE PROCESSOR, METHOD FOR PERFORMING DIGITAL SIGNAL PROCESSING BY USING THE PROGRAMMABLE PROCESSOR AND ITS IMPROVEMENT	
8	JP 07152 733 A	<input checked="" type="checkbox"/>	COMPUTER SYSTEM AND METHOD FOR PROCESSING VECTOR DATA	
9	JP 06323 894 A	<input checked="" type="checkbox"/>	WEIGHT MEASURING EQUIPMENT FOR LOADED VEHICLE	
10	JP 05342 185 A	<input checked="" type="checkbox"/>	CPU TIMER CONTROL SYSTEM	
11	JP 05233 279 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR	
12	JP 05197 743 A	<input checked="" type="checkbox"/>	VECTOR PROCESSOR	
13	JP 04156 620 A	<input checked="" type="checkbox"/>	VIRTUAL COMPUTER SYSTEM	
14	JP 04080 862 A	<input checked="" type="checkbox"/>	CIRCUIT RESET SYSTEM AT MACHINE CHECK	
15	JP 03261 817 A	<input checked="" type="checkbox"/>	CONTROLLING METHOD FOR STYLUS OF COORDINATE MEASURING MACHINE	
16	JP 02136 966 A	<input checked="" type="checkbox"/>	CLOCK STOP CONTROL SYSTEM ADAPTING MACHINE CHECK	
17	JP 02033 663 A	<input checked="" type="checkbox"/>	MACHINE CHECK PROCESSING SYSTEM	
18	JP 01073 875 A	<input checked="" type="checkbox"/>	METHOD AND DEVICE FOR CODING IMAGE DATA	
19	JP 63253 468 A	<input checked="" type="checkbox"/>	VECTOR PROCESSOR	
20	JP 63193 259 A	<input checked="" type="checkbox"/>	INSTRUCTION CONTROL SYSTEM FOR MULTIPROCESSOR	
21	JP 62198 960 A	<input checked="" type="checkbox"/>	VECTOR ARITHMETIC PROCESSOR	
22	JP 61080 451 A	<input checked="" type="checkbox"/>	VECTOR PROCESSOR	

	Document ID	U	Title	Current OR
23	JP 61025 274 A	<input checked="" type="checkbox"/>	VECTOR ARITHMETIC PROCESSOR	
24	JP 59106 075 A	<input checked="" type="checkbox"/>	DATA PROCESSING SYSTEM	
25	JP 57109 084 A	<input checked="" type="checkbox"/>	SCHEDULE SYSTEM FOR INSTRUCTION IN PARALLEL COMPUTER HAVING PLURAL OPERATING DEVICES	
26	GB 23904 43 A	<input checked="" type="checkbox"/>	A processor where some registers are not available to compiler generated code	
27	DE 19735 349 A1	<input checked="" type="checkbox"/>	Multiple data processor with single instruction combining vector and scalar operations	
28	EP 71882 2 A2	<input checked="" type="checkbox"/>	A low rate multi-mode CELP CODEC that uses backward prediction	
29	EP 68123 6 A1	<input checked="" type="checkbox"/>	Space vector data path.	
30	EP 64687 7 A2	<input checked="" type="checkbox"/>	Computer system and method for processing vector data.	
31	EP 44757 5 A1	<input checked="" type="checkbox"/>	A method for calculating scalar products of vectors by combining their elements.	
32	EP 35919 2 A2	<input checked="" type="checkbox"/>	Vector processors and vector register control.	
33	EP 10512 5 A2	<input checked="" type="checkbox"/>	Data processing system.	
34	NN780 7790	<input checked="" type="checkbox"/>	Execution of Intermediate Level Code From Multiple Address Spaces, with Application to a Shared Variable Language Processor in APL. July 1978.	
35	GB 23904 43 A	<input checked="" type="checkbox"/>	Microprocessor core with scalar and vector units for e.g. graphics processor, has execution unit and two sets of registers, with one register set not accessible to compiler-generated code but exclusively available to applications program	
36	GB 23826 72 A	<input checked="" type="checkbox"/>	Repeated instruction execution of operation defined by pair of values in image or multimedia processor uses repeat control unit to cause repeated execution of operations	
37	US 20030 03722 1 A	<input checked="" type="checkbox"/>	Microprocessor performs single vector operation on several data elements in parallel, and scalar operation on data element, during respective_vector_and_scalar_operation_modes ..	
38	US 64836 06 B	<input checked="" type="checkbox"/>	Ink colorant selection method for inkjet printer, involves performing scalar and vector error diffusion processes on respective portions of source color that is divided by performing undercolor removal process	
39	JP 20020 97724 A	<input checked="" type="checkbox"/>	Setting method for shaped steel member juncture of curved structure e.g. curved roof, involves calculating normal line vector from central node to each surrounding nodes	
40	US 20010 04746 9 A	<input checked="" type="checkbox"/>	Machine readable medium for computer system, stores instructions for operating shared architecturally visible register file as flat register file during execution of packed and scalar floating point instructions	
41	US 62666 86 B	<input checked="" type="checkbox"/>	Execution of floating point and packed data instructions by a processor, involves altering data to indicate that stack is empty in response to execution of the single transition instruction	
42	JP 20011 95390 A	<input checked="" type="checkbox"/>	Operand cache for vector processor in computer system, has selector to choose output from scalar data area when input address is within predetermined area of main memory	

	Document ID	U	Title	Current OR
43	EP 10110 52 A	<input checked="" type="checkbox"/>	Processing system with shared memory type vector to run applications with vector and scalar resources by setting central processing units (CPU) as master scalar processing unit accompanied by slave operating multi-vector pipeline units	
44	JP 20000 27066 A	<input checked="" type="checkbox"/>	Formation method of moire pattern on decorative sheets, involves forming false pattern based on two dimensional scalar field and adjusting pattern which is converted to vector mode with respect to control point	
45	US 59266 43 A	<input checked="" type="checkbox"/>	Data driven processor for performing parallel scalar and vector processing	
46	EP 10254 85 B	<input checked="" type="checkbox"/>	Microprocessor for performing multimedia extension or 3D graphic instructions	
47	JP 11025 072 A	<input checked="" type="checkbox"/>	Information processor of multi processor system - has pair of scalar processors connected with vector processors that shares interface between main memory	
48	JP 10207 720 A	<input checked="" type="checkbox"/>	Information processor with provision for operating in scalar and vector modes - has controller that switches operational mode to scalar and vector modes during which scalar and vector instructions are executed using pair of register sets as scalar and vector register sets	
49	FR 27526 29 A	<input checked="" type="checkbox"/>	Multiple data processor with single instruction combining vector and scalar operations - has both scalar registers and vector registers and combines scalar and vector processing as required to speed processing of multimedia data	
50	JP 09282 308 A	<input checked="" type="checkbox"/>	Vector instruction control system for LSI in information processor, microprocessor - has vector unit which executes vector instruction of short length of LSI chip which is built in vector unit	
51	JP 08305 489 A	<input checked="" type="checkbox"/>	Joystick drive appts used in 3D co-ordinates measurement machine - computes scalar product of each digital signal and each direction vector of unit to obtain drive vector which is applied to drive motors	
52	US 55617 84 A	<input checked="" type="checkbox"/>	Accessing common memory in cluster architecture for highly parallel multiprocessor scalar-factor computer - determining if logical address is within start and end range as defined by segment registers and relocating logical address to physical address using displacement value in another segment register	
53	US 55376 06 A	<input checked="" type="checkbox"/>	Scalar pipeline replication for parallel vector element processing - executes scalar instructions to operate as vector processor when vector length register contains non-zero value, and to operate as scalar processor when vector length register contains zero value	
54	EP 71882 2 A	<input checked="" type="checkbox"/>	Low rate multi-mode code excited linear predictive coding device using backward prediction - determining set of non-quantised line-spectral-frequencies-to-represent-short term predictor parameters for partic. segment, and applying mode specific scalar or vector quantisation	
55	US 55112 17 A	<input checked="" type="checkbox"/>	Multiple operating system running method on virtual machine for e.g supercomputer - by assigning vector processing tasks from any of virtual machines to vector processor which are shared among operating systems running on scalar processor	
56	EP 68123 6 A	<input checked="" type="checkbox"/>	Programmable processor for space vector data path to integrate SIMD into general purpose programmable processor - specifies whether each instruction is in either vector or scalar mode and sends signal to processing unit	
57	US 54370 43 A	<input checked="" type="checkbox"/>	Information processing system with interchangeable register windows - has number of registers configurable as scalar registers constituting register windows or element registers of vector registers designated by instruction using vector registers	
58	US 54267 54 A	<input checked="" type="checkbox"/>	Combined scalar and vector processing system - has scalar XI directory recording lines currently being stored by scalar processors, and vector store registers recording lines currently being stored into by vector processors	

	Document ID	U	Title	Current OR
59	EP 64687 7 A	<input checked="" type="checkbox"/>	Scalar computer with vector data processing facility - has multi-element vector registers controlled to sequence transfer of vector data between main memory and processing unit of scalar computer sequentially	
60	WO 94130 66 A	<input checked="" type="checkbox"/>	Dot product circuit for multipath receiver for cellular telephone QPSK demodulation signal weighting - calculates scalar projection by multiplying first component of first and second vectors, and second component of first and second vectors, to produce intermediate value for summing in accumulator	
61	DE 43080 83 C	<input checked="" type="checkbox"/>	Scalar or vector value generation for fuzzy logic controller - processing measurement valves in two stages using respective fuzzy logic modules and inference devices, and hyper-fuzzification module	
62	EP 59098 0 B	<input checked="" type="checkbox"/>	Image data processing appts. for multi-dimensional data - calculating lighting characteristics in response to lighting parameters of surfaces and parameters of light sources, where surface highlight characteristics produced by non-linear process	
63	EP 55315 8 B	<input checked="" type="checkbox"/>	Scalable multiprocessor supercomputer adapted for vector processing - has multithreaded context switching processor that covers memory access latencies by executing unrelated code from multiple program threads	
64	EP 47843 1 A	<input checked="" type="checkbox"/>	Digital signal coding for scalar product determination of 2 vectors - uses formation of partial sums of products and interconnection matrix driven by encoder, then combines partial partial results	
65	JP 04063 001 A	<input checked="" type="checkbox"/>	Impedance matching method - controlling scalar product of electric field and mode vector generated as standing wave in cavity resonator NoAbstract Dwg 1/3	
66	EP 44757 5 A	<input checked="" type="checkbox"/>	Calculation of scalar products of vectors by combining elements - to produce partial products which may be used again later in other calculate loss without regeneration to same time	
67	EP 51200 7 B	<input checked="" type="checkbox"/>	Highly parallel multiprocessor computer cluster architecture - has clusters of tightly-coupled high speed processors accessing shared resources of associated and other clusters	
68	US 49640 35 A	<input checked="" type="checkbox"/>	Vector processing system - has shared store accessible by resources of scalar and vector processors without address translation processing	
69	EP 38705 1 A	<input checked="" type="checkbox"/>	Coding image information and creating code book - divides digital information into pixel blocks and subjects picture information to vector quantisation in block units	
70	CA 20101 00 A	<input checked="" type="checkbox"/>	Measuring AC power as scalar and vector quantity - decomposing measured voltage and current values into orthogonal components and combining to give power values	
71	EP 35919 2-A	<input checked="" type="checkbox"/>	Vector register control for more efficient computer operation - using memory modules identified by new address number produced-by-combining-address-number-and-scaler-unit-number	
72	EP 34849 5 B	<input checked="" type="checkbox"/>	Main memory and cache system for vector and scalar processors - provides efficient use of cache by vector processor by pre-loading vector data blocks into cache memory	
73	EP 11430 4 A	<input checked="" type="checkbox"/>	Vector processing hardware assist appts. - is for digital processor using cache memory to have vector operand elements read from it and operation results written into it	
74	EP 37164 A	<input type="checkbox"/>	Self-organising pattern class separator and identifier - has assemblies with matrix of junction elements receiving vector component signals scalar multiplied in training mode and threshold detected	

	Document ID	U	Title	Current OR
1	US 20030 03722 1 A1	<input type="checkbox"/>	Processor implementation having unified scalar and SIMD datapath	712/3
2	US 20030 02364 6 A1	<input checked="" type="checkbox"/>	Processor capable of executing packed shift operations	708/209
3	US 20020 03284 8 A1	<input type="checkbox"/>	Method and apparatus for obtaining a scalar value directly from a vector register	712/4
4	US 62437 62 B1	<input checked="" type="checkbox"/>	Methods and apparatus for data access and program generation on a multiprocessing computer	719/310
5	US 60852 75 A	<input type="checkbox"/>	Data processing system and method thereof	710/316
6	US 60471 22 A	<input type="checkbox"/>	System for method for performing a context switch operation in a massively parallel computer system	718/108
7	US 60163 95 A	<input type="checkbox"/>	Programming a vector processor and parallel programming of an asymmetric dual multiprocessor comprised of a vector processor and a risc processor	717/149
8	US 58058 74 A	<input type="checkbox"/>	Method and apparatus for performing a vector skip instruction in a data processor	712/222
9	US 57548 05 A	<input type="checkbox"/>	Instruction in a data processing system utilizing extension bits and method therefor	712/200
10	US 57520 74 A	<input type="checkbox"/>	Data processing system and method thereof	712/29
11	US 57427 86 A	<input type="checkbox"/>	Method and apparatus for storing vector data in multiple non-consecutive locations in a data processor using a mask value	711/217
12	US 57402 83 A	<input type="checkbox"/>	Digital video compression utilizing mixed vector and scalar outputs	382/248
13	US 57375 86 A	<input type="checkbox"/>	Data processing system and method thereof	712/236
14	US 57348 79 A	<input type="checkbox"/>	Saturation instruction in a data processor	712/221
15	US 57179 47 A	<input type="checkbox"/>	Data processing system and method thereof	712/3
16	US 57064 88 A	<input type="checkbox"/>	Data processing system and method thereof	712/223
17	US 56641 34 A	<input type="checkbox"/>	Data processor for performing a comparison instruction using selective enablement and wired boolean logic	712/245
18	US 56008 46 A	<input type="checkbox"/>	Data processing system and method thereof	712/5
19	US 55985 71 A	<input type="checkbox"/>	Data processor for conditionally modifying extension bits in response to data processing instruction execution	712/9
20	US 55726 89 A	<input type="checkbox"/>	Data processing system and method thereof	712/200
21	US 55599 73 A	<input type="checkbox"/>	Data processing system and method thereof	712/241
22	US 55487 68 A	<input type="checkbox"/>	Data processing system and method thereof	712/200

	Document ID	U	Title	Current OR
23	US 55375 62 A	<input type="checkbox"/>	Data processing system and method thereof	712/234
24	US 54758 49 A	<input checked="" type="checkbox"/>	Memory control device with vector processors and a scalar processor	712/6
25	US 53613 63 A	<input type="checkbox"/>	Input/output system for parallel computer for performing parallel file transfers between selected number of input/output devices and another selected number of processing nodes	712/22
26	US 53534 12 A	<input type="checkbox"/>	Partition control circuit for separately controlling message sending of nodes of tree-shaped routing network to divide the network into a number of partitions	709/243
27	US 50739 70 A	<input type="checkbox"/>	Vector processing apparatus allowing succeeding vector instruction chain processing upon completion of decoding of a preceding vector instruction chain	712/7
28	US 50634 97 A	<input checked="" type="checkbox"/>	Apparatus and method for recovering from missing page faults in vector data processing operations	712/6
29	US 49910 83 A	<input checked="" type="checkbox"/>	Method and system for extending address space for vector processing	711/207
30	US 49741 45 A	<input checked="" type="checkbox"/>	Processor system including a paging processor for controlling paging between a main storage and an extended storage	712/6
31	US 49338 39 A	<input checked="" type="checkbox"/>	Vector processor	712/8
32	US 48377 30 A	<input type="checkbox"/>	Linking scalar results directly to scalar operation inputs on a bidirectional databus in a computer which superpositions vector and scalar operations	712/7
33	US 47775 93 A	<input type="checkbox"/>	Vector processing apparatus including means for identifying the occurrence of exceptions in the processing of vector elements	712/9
34	US 46333 89 A	<input type="checkbox"/>	Vector processor system comprised of plural vector processors	712/4

	L #	Hits	Search Text	DBs
1	L1	396	(shar\$3 common unified united combin\$3 mode) near20 (scalar near10 (vector pack\$3 simd))	USPAT; US-PGPUB
2	L2	9791	(tag bit field flag indicat\$3 identif\$6) near30 ((activ\$5 valid\$4 enabl\$3 disabl\$3 invalid\$4 set\$4) near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	USPAT; US-PGPUB
3	L3	72	1 and 2	USPAT; US-PGPUB
4	L5	1285	(tag bit field flag indicat\$3 identif\$6) near30 ((activ\$5 valid\$4 enabl\$3 disabl\$3 invalid\$4 set\$4) near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	EPO; JPO; DERWENT; IBM_TDB
5	L6	0	4 and 5	EPO; JPO; DERWENT; IBM_TDB
6	L4	74	(shar\$3 common unified united combin\$3 mode) near20 (scalar near10 (vector pack\$3 simd))	EPO; JPO; DERWENT; IBM_TDB
7	L9	34	2 near30 scalar	USPAT; US-PGPUB
8	L10	1	5 near30 scalar	EPO; JPO; DERWENT; IBM_TDB
9	L11	47858	(tag bit field flag indicat\$3 identif\$6) near10 ((data datum subdata portion part\$3 section segment sub) near10 register)	USPAT; US-PGPUB
10	L12	290	11 near30 ((activ\$5 valid\$4 enabl\$3 disabl\$3 invalid\$4 set\$4) near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	USPAT; US-PGPUB
11	L13	22	12 and (scalar near20 (vector pack\$3 simd))	USPAT; US-PGPUB
12	L16	15045	(tag bit field flag indicat\$3 identif\$6) near10 ((data datum subdata portion part\$3 section segment sub) near10 register)	EPO; JPO; DERWENT; IBM_TDB
13	L17	33	16 near30 ((activ\$5 valid\$4 enabl\$3 disabl\$3 invalid\$4 set\$4) near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	EPO; JPO; DERWENT; IBM_TDB
14	L18	0	17 and (scalar near20 (vector pack\$3 simd))	EPO; JPO; DERWENT; IBM_TDB
15	L19	145	1 and ((activ\$5 valid\$4 enabl\$3 disabl\$3 invalid\$4 set\$4) near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	USPAT; US-PGPUB
16	L20	73	19 not (3 13)	USPAT; US-PGPUB
17	L21	39	1 near10 ((function\$3 operation\$3 process\$3) adj2 (element unit module block))	USPAT; US-PGPUB
18	L24	89	(scalar near10 (vector SIMD packed)) near20 (alu (datapath (data adj1 path)) ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	EPO; JPO; DERWENT; IBM_TDB
19	L22	371	(scalar near10 (vector SIMD packed)) near20 (alu (datapath (data adj1 path)) ((function\$3 operation\$3 process\$3) adj2 (element unit module block)))	USPAT; US-PGPUB
20	L26	198	(scalar near10 (vector SIMD packed)) near20 (alu (datapath (data adj1 path)) ((function\$3 operation\$3 adj2 (unit module block)))	USPAT; US-PGPUB
21	L27	173	22 not 26	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	US 20040 02480 0 A1	<input type="checkbox"/>	Method and apparatus for performing packed shift operations	708/209
2	US 20040 01974 7 A1	<input checked="" type="checkbox"/>	Narrow/wide cache	711/141
3	US 20040 01568 2 A1	<input checked="" type="checkbox"/>	Application registers	712/228
4	US 20040 01567 7 A1	<input checked="" type="checkbox"/>	Digital signal processor with SIMD organization and flexible data manipulation	712/22
5	US 20040 00320 6 A1	<input checked="" type="checkbox"/>	STREAMING VECTOR PROCESSOR WITH RECONFIGURABLE INTERCONNECTION SWITCH	712/218
6	US 20030 20042 6 A1	<input checked="" type="checkbox"/>	System for expanded instruction encoding and method thereof	712/241
7	US 20030 18956 5 A1	<input checked="" type="checkbox"/>	Single semiconductor graphics platform system and method with skinning, swizzling and masking capabilities	345/418
8	US 20030 17425 2 A1	<input checked="" type="checkbox"/>	Programmable motion estimation module with vector array unit	348/699
9	US 20030 16484 0 A1	<input checked="" type="checkbox"/>	High quality antialiased lines with dual sampling pattern	345/611
10	US 20030 16483 0 A1	<input checked="" type="checkbox"/>	Yield enhancement of complex chips	345/505
11	US 20030 16482 5 A1	<input checked="" type="checkbox"/>	In-circuit test using scan chains	345/419
12	US 20030 16482 4 A1	<input checked="" type="checkbox"/>	Graphics engine with isochronous context switching	345/419
13	US 20030 16482 3 A1	<input checked="" type="checkbox"/>	3D graphics accelerator architecture	345/419
14	US 20030 16367 1 A1	<input checked="" type="checkbox"/>	Method and apparatus for prioritized instruction issue queue	712/214
15	US 20030 16366 7 A1	<input checked="" type="checkbox"/>	Vector processing system	712/7
16	US 20030 15902 3 A1	<input checked="" type="checkbox"/>	Repeated instruction execution	712/241
17	US 20030 15901 7 A1	<input checked="" type="checkbox"/>	Data access in a processor	712/34

	Document ID	U	Title	Current OR
18	US 20030 15901 6 A1	<input checked="" type="checkbox"/>	Data access in a processor	712/4
19	US 20030 15436 1 A1	<input checked="" type="checkbox"/>	Instruction execution in a processor	712/214
20	US 20030 15214 8 A1	<input checked="" type="checkbox"/>	System and method for multiple channel video transcoding	375/240 .24
21	US 20030 11550 0 A1	<input checked="" type="checkbox"/>	Processor with redundant logic	714/10
22	US 20030 11224 6 A1	<input checked="" type="checkbox"/>	Blending system and method in an integrated computer graphics pipeline	345/519
23	US 20030 11224 5 A1	<input checked="" type="checkbox"/>	Single semiconductor graphics platform	345/506
24	US 20030 10305 4 A1	<input checked="" type="checkbox"/>	Integrated graphics processing unit with antialiasing	345/506
25	US 20030 10305 0 A1	<input checked="" type="checkbox"/>	Masking system and method for a graphics processing framework embodied on a single semiconductor platform	345/426
26	US 20030 07909 0 A1	<input checked="" type="checkbox"/>	Instructions for test & set with selectively enabled cache invalidate	711/140
27	US 20030 03880 8 A1	<input checked="" type="checkbox"/>	Method, apparatus and article of manufacture for a sequencer in a transform/lighting module capable of processing multiple independent execution threads	345/506
28	US 20030 03722 1 A1	<input checked="" type="checkbox"/>	Processor implementation having unified scalar and SIMD datapath	712/3
29	US 20030 03497 5 A1	<input checked="" type="checkbox"/>	Lighting system and method for a graphics processor	345/426
30	US 20030 03450 2 A1	<input checked="" type="checkbox"/>	Structure and method for fabricating semiconductor structures having memory systems with pre-computation units, utilizing the formation of a compliant substrate	257/140
31	US 20030 02364 6 A1	<input checked="" type="checkbox"/>	Processor capable of executing packed shift operations	708/209
32	US 20030 02072 0 A1	<input checked="" type="checkbox"/>	Method, apparatus and article of manufacture for a sequencer in a transform/lighting module capable of processing multiple independent execution threads	345/506
33	US 20030 01867 6 A1	<input checked="" type="checkbox"/>	Multi-function floating point arithmetic pipeline	708/501
34	US 20030 01621 7 A1	<input checked="" type="checkbox"/>	Method and apparatus for processing non-planar video graphics primitives	345/423

	Document ID	U	Title	Current OR
35	US 20030 01244 3 A1	<input checked="" type="checkbox"/>	Method and apparatus for encoding and decoding images	382/232
36	US 20030 01159 5 A1	<input checked="" type="checkbox"/>	Apparatus for processing non-planar video graphics primitives and associated method of operation	345/423
37	US 20020 19625 9 A1	<input checked="" type="checkbox"/>	Single semiconductor graphics platform with blending and fog capabilities	345/506
38	US 20020 18074 0 A1	<input checked="" type="checkbox"/>	Clipping system and method for a single graphics semiconductor platform	345/506
39	US 20020 15747 8 A1	<input checked="" type="checkbox"/>	System and method for quantifying material properties	73/789
40	US 20020 13088 6 A1	<input checked="" type="checkbox"/>	Antialias mask generation	345/611
41	US 20020 13087 4 A1	<input checked="" type="checkbox"/>	Vector instruction set	345/506
42	US 20020 13086 3 A1	<input checked="" type="checkbox"/>	Tile relative origin for plane equations	345/420
43	US 20020 12612 6 A1	<input checked="" type="checkbox"/>	Parameter circular buffers	345/557
44	US 20020 12612 4 A1	<input checked="" type="checkbox"/>	Planar byte memory organization with linear access	345/533
45	US 20020 11820 2 A1	<input checked="" type="checkbox"/>	Same tile method	345/530
46	US 20020 11659 5 A1	<input checked="" type="checkbox"/>	Digital signal processor integrated circuit	712/22
47	US 20020 10551 9 A1	<input checked="" type="checkbox"/>	Clipping system and method for a graphics processing framework embodied on a single semiconductor platform	345/426
48	US 20020 06934 5 A1	<input checked="" type="checkbox"/>	High performance VLIW processor	712/215
49	US 20020 04784 6 A1	<input checked="" type="checkbox"/>	System, method and computer program product for performing a scissor operation in a graphics processing framework embodied on a single semiconductor platform	345/522
50	US 20020 02755 3 A1	<input checked="" type="checkbox"/>	Diffuse-coloring system and method for a graphics processing framework embodied on a single semiconductor platform	345/426
51	US 20010 01762 6 A1	<input checked="" type="checkbox"/>	Graphics processing unit with transform module capable of handling scalars and vectors	345/501

	Document ID	U	Title	Current OR
52	US 20010 01686 1 A1	<input checked="" type="checkbox"/>	Apparatus for performing packed shift operations	708/209
53	US 20010 00758 2 A1	<input checked="" type="checkbox"/>	Data transmitting apparatus, automatic level adjustment method and activation control method	375/316
54	US 20010 00520 9 A1	<input checked="" type="checkbox"/>	Method, apparatus and article of manufacture for a transform module in a graphics processor	345/506
55	US 67005 81 B2	<input checked="" type="checkbox"/>	In-circuit test using scan chains	345/519
56	US 66752 85 B1	<input checked="" type="checkbox"/>	Geometric engine including a computational module without memory contention	712/201
57	US 66649 60 B2	<input checked="" type="checkbox"/>	Apparatus for processing non-planar video graphics primitives and associated method of operation	345/423
58	US 66544 99 B2	<input checked="" type="checkbox"/>	Method and apparatus for encoding and decoding images	382/232
59	US 66503 31 B2	<input checked="" type="checkbox"/>	System, method and computer program product for performing a scissor operation in a graphics processing framework embodied on a single semiconductor platform	345/522
60	US 66503 30 B2	<input checked="" type="checkbox"/>	Graphics system and method for processing multiple independent execution threads	345/506
61	US 66503 25 B1	<input checked="" type="checkbox"/>	Method, apparatus and article of manufacture for boustrophedonic rasterization	345/426
62	US 66402 99 B1	<input checked="" type="checkbox"/>	Method and apparatus for arbitrating access to a computational engine for use in a video graphics controller	712/245
63	US 66316 47 B2	<input checked="" type="checkbox"/>	System and method for quantifying material properties	73/789
64	US 66313 89 B2	<input checked="" type="checkbox"/>	Apparatus for performing packed shift operations	708/209
65	US 66309 35 B1	<input checked="" type="checkbox"/>	Geometric engine including a computational module for use in a video graphics controller	345/522
66	US 66292 31 B1	<input checked="" type="checkbox"/>	System and method for efficient register file conversion of denormal numbers between scalar and SIMD formats	712/1
67	US 66248 18 B1	<input checked="" type="checkbox"/>	Method and apparatus for shared microcode in a multi-thread computation engine	345/522
68	US 65973 56 B1	<input checked="" type="checkbox"/>	Integrated tessellator in a graphics processing unit	345/423
69	US 65913 45 B1	<input checked="" type="checkbox"/>	Method for ensuring maximum bandwidth on accesses to strided vectors in a bank-interleaved cache	711/127
70	US 65773 09 B2	<input checked="" type="checkbox"/>	System and method for a graphics processing framework embodied utilizing a single semiconductor platform	345/426
71	US 65739 00 B1	<input checked="" type="checkbox"/>	Method, apparatus and article of manufacture for a sequencer in a transform/lighting module capable of processing multiple independent execution threads	345/537
72	US 65670 84 B1	<input checked="" type="checkbox"/>	Lighting effect computation circuit and method therefore	345/426
73	US 65300 11 B1	<input checked="" type="checkbox"/>	Method and apparatus for vector register with scalar values	712/3

	Document ID	U	Title	Current OR
74	US 65156 71 B1	<input checked="" type="checkbox"/>	Method, apparatus and article of manufacture for a vertex attribute buffer in a graphics processor	345/506
75	US 65045 42 B1	<input checked="" type="checkbox"/>	Method, apparatus and article of manufacture for area rasterization using sense points	345/441
76	US 64774 81 B1	<input checked="" type="checkbox"/>	Device and method for outputting stochastic processes, and data recording medium	702/179
77	US 64627 37 B2	<input checked="" type="checkbox"/>	Clipping system and method for a graphics processing framework embodied on a single semiconductor platform	345/426
78	US 64525 95 B1	<input checked="" type="checkbox"/>	Integrated graphics processing unit with antialiasing	345/426
79	US 64178 51 B1	<input checked="" type="checkbox"/>	Method and apparatus for lighting module in a graphics processor	345/426
80	US 64008 47 B1	<input checked="" type="checkbox"/>	Method and apparatus for encoding and decoding images	382/232
81	US 63669 98 B1	<input checked="" type="checkbox"/>	Reconfigurable functional units for implementing a hybrid VLIW-SIMD programming model	712/17
82	US 63534 39 B1	<input checked="" type="checkbox"/>	System, method and computer program product for a blending operation in a transform module of a computer graphics pipeline	345/561
83	US 63428 88 B1	<input checked="" type="checkbox"/>	Graphics processing unit with an integrated fog and blending operation	345/426
84	US 63178 19 B1	<input checked="" type="checkbox"/>	Digital signal processor containing scalar processor and a plurality of vector processors operating from a single instruction	712/22
85	US 62984 38 B1	<input checked="" type="checkbox"/>	System and method for conditional moving an operand from a source register to destination register	712/226
86	US 62758 34 B1	<input checked="" type="checkbox"/>	Apparatus for performing packed shift operations	708/209
87	US 62667 59 B1	<input checked="" type="checkbox"/>	Register scoreboard to support overlapped execution of vector memory reference instructions in a vector processor	712/5
88	US 62634 17 B1	<input checked="" type="checkbox"/>	Method of implementing vector operation using a processor chip which is provided with a vector unit	712/34
89	US 61984 88 B1	<input checked="" type="checkbox"/>	Transform, lighting and rasterization system embodied on a single semiconductor platform	345/426
90	US 61956 76 B1	<input checked="" type="checkbox"/>	Method and apparatus for user side scheduling in a multiprocessor operating system program that implements distributive scheduling of processes	718/107
91	US 61733 66 B1	<input checked="" type="checkbox"/>	Load and store instructions which perform unpacking and packing of data bits in separate vector and integer cache storage	711/129
92	US 61548 31 A	<input checked="" type="checkbox"/>	Decoding operands for multimedia applications instruction coded with less number of bits than combination of register slots and selectable specific values	712/208
93	US 61449 80 A	<input checked="" type="checkbox"/>	Method and apparatus for performing multiple types of multiplication including signed and unsigned multiplication	708/627
94	US 61447 71 A	<input checked="" type="checkbox"/>	Method and apparatus for encoding and decoding images	382/239
95	US 61416 73 A	<input checked="" type="checkbox"/>	Microprocessor modified to perform inverse discrete cosine transform operations on a one-dimensional matrix of numbers within a minimal number of instructions	708/402
96	US 60887 83 A	<input checked="" type="checkbox"/>	DPS having a plurality of like processors controlled in parallel by an instruction word, and a control processor also controlled by the instruction word	712/22

	Document ID	U	Title	Current OR
97	US 60615 21 A	<input checked="" type="checkbox"/>	Computer having multimedia operations executable as two distinct sets of operations within a single instruction cycle	712/9
98	US 60584 65 A	<input checked="" type="checkbox"/>	Single-instruction-multiple-data processing in a multimedia signal processor	712/7
99	US 60527 71 A	<input checked="" type="checkbox"/>	Microprocessor with pipeline synchronization	712/34
100	US 60473 72 A	<input checked="" type="checkbox"/>	Apparatus for routing one operand to an arithmetic logic unit from a fixed register slot and another operand from any register slot	712/222
101	US 60473 67 A	<input checked="" type="checkbox"/>	Microprocessor with improved out of order support	712/23
102	US 60163 95 A	<input checked="" type="checkbox"/>	Programming a vector processor and parallel programming of an asymmetric dual multiprocessor comprised of a vector processor and a risc processor	717/149
103	US 60095 05 A	<input checked="" type="checkbox"/>	System and method for routing one operand to arithmetic logic units from fixed register slots and another operand from any register slot	712/6
104	US 60063 15 A	<input checked="" type="checkbox"/>	Computer methods for writing a scalar value to a vector	712/7
105	US 59833 36 A	<input checked="" type="checkbox"/>	Method and apparatus for packing and unpacking wide instruction word using pointers and masks to shift word syllables to designated execution units groups	712/24
106	US 59788 38 A	<input checked="" type="checkbox"/>	Coordination and synchronization of an asymmetric, single-chip, dual multiprocessor	709/208
107	US 59494 10 A	<input checked="" type="checkbox"/>	Apparatus and method for synchronizing audio and video frames in an MPEG presentation system	715/500 .1
108	US 59419 38 A	<input checked="" type="checkbox"/>	System and method for performing an accumulate operation on one or more operands within a partitioned register	708/490
109	US 59406 25 A	<input checked="" type="checkbox"/>	Density dependent vector mask operation control apparatus and method	712/5
110	US 59238 62 A	<input checked="" type="checkbox"/>	Processor that decodes a multi-cycle instruction into single-cycle micro-instructions and schedules execution of the micro-instructions	712/208
111	US 59095 72 A	<input checked="" type="checkbox"/>	System and method for conditionally moving an operand from a source register to a destination register	712/226
112	US 59092 24 A	<input checked="" type="checkbox"/>	Apparatus and method for managing a frame buffer for MPEG video decoding in a PC environment	345/531
113	US 59037 69 A	<input checked="" type="checkbox"/>	Conditional vector processing	712/5
114	US 58955 01 A	<input checked="" type="checkbox"/>	Virtual memory system for vector based computer systems	711/207
115	US 58931 45 A	<input checked="" type="checkbox"/>	System and method for routing operands within partitions of a source register to partitions within a destination register	711/125
116	US 58930 66 A	<input checked="" type="checkbox"/>	Fast requantization apparatus and method for MPEG audio decoding	704/500
117	US 58871 86 A	<input checked="" type="checkbox"/>	Method of solving simultaneous linear equations in a memory-distributed parallel computer	712/28
118	US 58389 84 A	<input checked="" type="checkbox"/>	Single-instruction-multiple-data processing using multiple banks of vector registers	712/5
119	US 58359 71 A	<input checked="" type="checkbox"/>	Method and apparatus for generating addresses in parallel processing systems	711/220

	Document ID	U	Title	Current OR
120	US 58226 06 A	<input checked="" type="checkbox"/>	DSP having a plurality of like processors controlled in parallel by an instruction word, and a control processor also controlled by the instruction word	712/16
121	US 58187 39 A	<input checked="" type="checkbox"/>	Processor for performing shift operations on packed data	708/209
122	US 58058 75 A	<input checked="" type="checkbox"/>	Vector processing system with multi-operation, run-time configurable pipelines	712/222
123	US 58019 75 A	<input checked="" type="checkbox"/>	Computer modified to perform inverse discrete cosine transform operations on a one-dimensional matrix of numbers within a minimal number of instruction cycles	708/402
124	US 57782 41 A	<input checked="" type="checkbox"/>	Space vector data path	712/20
125	US 57457 21 A	<input checked="" type="checkbox"/>	Partitioned addressing apparatus for vector/scalar registers	712/208
126	US 57402 83 A	<input checked="" type="checkbox"/>	Digital video compression utilizing mixed vector and scalar outputs	382/248
127	US 57178 81 A	<input checked="" type="checkbox"/>	Data processing system for processing one and two parcel instructions	712/205
128	US 57064 90 A	<input checked="" type="checkbox"/>	Method of processing conditional branch instructions in scalar/vector processor	712/234
129	US 56662 98 A	<input checked="" type="checkbox"/>	Method for performing shift operations on packed data	708/209
130	US 56597 06 A	<input checked="" type="checkbox"/>	Vector/scalar processor with simultaneous processing and instruction cache filling	711/125
131	US 56447 48 A	<input checked="" type="checkbox"/>	Processor system including an index buffer circuit and a translation look-aside buffer control circuit for processor-to-processor interfacing	711/207
132	US 56405 24 A	<input checked="" type="checkbox"/>	Method and apparatus for chaining vector instructions	712/222
133	US 56236 50 A	<input checked="" type="checkbox"/>	Method of processing a sequence of conditional vector IF statements	712/234
134	US 55985 47 A	<input checked="" type="checkbox"/>	Vector processor having functional unit paths of differing pipeline lengths	712/222
135	US 55814 90 A	<input checked="" type="checkbox"/>	Contact management model assessment system for contact tracking in the presence of model uncertainty and noise	703/2
136	US 55618 08 A	<input checked="" type="checkbox"/>	Asymmetric vector multiprocessor composed of a vector unit and a plurality of scalar units each having a different architecture	712/3
137	US 55617 84 A	<input checked="" type="checkbox"/>	Interleaved memory access system having variable-sized segments logical address spaces and means for dividing/mapping physical address into higher and lower order addresses	711/157
138	US 55443 37 A	<input checked="" type="checkbox"/>	Vector processor having registers for control by vector registers	712/4
139	US 55376 06 A	<input checked="" type="checkbox"/>	Scalar pipeline replication for parallel vector element processing	712/7
140	US 55308 81 A	<input checked="" type="checkbox"/>	Vector processing apparatus for processing different instruction set architectures corresponding to mingled-type programs and separate-type programs	712/7
141	US 55176 66 A	<input checked="" type="checkbox"/>	Program controlled processor wherein vector distributor and vector coupler operate independently of sequencer	712/3

	Document ID	U	Title	Current OR
142	US 54715 93 A	<input checked="" type="checkbox"/>	Computer processor with an efficient means of executing many instructions simultaneously	712/235
143	US 54370 43 A	<input checked="" type="checkbox"/>	Information processing apparatus having a register file used interchangeably both as scalar registers of register windows and as vector registers	712/1
144	US 54308 84 A	<input checked="" type="checkbox"/>	Scalar/vector processor	712/3
145	US 54249 61 A	<input checked="" type="checkbox"/>	Process and system for measuring the temporal course of a periodic signal having high time resolution according to a "Boxcar-like" process	702/57
146	US 54230 51 A	<input checked="" type="checkbox"/>	Execution unit with an integrated vector operation capability	712/7
147	US 54189 73 A	<input checked="" type="checkbox"/>	Digital computer system with cache controller coordinating both vector and scalar operations	712/3
148	US 53903 29 A	<input checked="" type="checkbox"/>	Responding to service requests using minimal system-side context in a multiprocessor environment	718/108
149	US 53815 36 A	<input checked="" type="checkbox"/>	Method and apparatus for separate mark and wait instructions for processors having multiple memory ports	711/168
150	US 53597 18 A	<input checked="" type="checkbox"/>	Early scalable instruction set machine alu status prediction apparatus	712/221
151	US 53496 77 A	<input checked="" type="checkbox"/>	Apparatus for calculating delay when executing vector tailgating instructions and using delay to facilitate simultaneous reading of operands from and writing of results to same vector register	712/4
152	US 53414 82 A	<input checked="" type="checkbox"/>	Method for synchronization of arithmetic exceptions in central processing units having pipelined execution units simultaneously executing instructions	712/244
153	US 53074 78 A	<input checked="" type="checkbox"/>	Method for inserting a path instruction during compilation of computer programs for processors having multiple functional units	703/22
154	US 52993 19 A	<input checked="" type="checkbox"/>	High performance interlock collapsing SCISM ALU apparatus	712/221
155	US 52936 02 A	<input checked="" type="checkbox"/>	Multiprocessor computer system with dedicated synchronizing cache	711/147
156	US 52915 81 A	<input checked="" type="checkbox"/>	Apparatus and method for synchronization of access to main memory signal groups in a multiprocessor data processing system	711/152
157	US 52788 40 A	<input checked="" type="checkbox"/>	Apparatus and method for data induced condition signalling	714/25
158	US 52611 13 A	<input checked="" type="checkbox"/>	Apparatus and method for single operand register array for vector and scalar data processing operations	712/8
159	US 52187 12 A	<input checked="" type="checkbox"/>	Providing a data processor with a user-mode accessible mode of operations in which the processor performs processing operations without interruption	710/261
160	US 52029 75 A	<input checked="" type="checkbox"/>	Method for optimizing instruction scheduling for a processor having multiple functional resources	717/151
161	US 51971 30 A	<input checked="" type="checkbox"/>	Cluster architecture for a highly parallel scalar/vector multiprocessor system	712/3
162	US 51877 96 A	<input checked="" type="checkbox"/>	Three-dimensional vector co-processor having I, J, and K register files and I, J, and K execution units	712/4
163	US 51797 02 A	<input checked="" type="checkbox"/>	System and method for controlling a highly parallel multiprocessor using an anarchy based scheduler for parallel execution thread scheduling	718/102